

**SEARCH REQUEST FORM****Scientific and Technical Information Center**

Requester's Full Name: Lynette T. Umez-Fronine Examiner #: 7498M Date: 4/13/01  
 Art Unit: 1765 Phone Number 305-9074 Serial Number: 9/895 6935  
 Mail Box and Bldg/Room Location: OE 12 Results Format Preferred (circle): PAPER DISK E-MAIL  
CP 3

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Method of Forming a Metal Wiring in A Semiconductor Device  
 Inventors (please provide full names): Sung Gyu Pyo

Earliest Priority Filing Date: 6/20/1999 US20020067277

\*For Sequence Searches Only\* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.

Search claim 1, using examples of

- i. diffusion prevention film spacer as recited in claim 5
- ii. chemical enhancer layers as in claims 7, ~~and~~ 8, 9, and 10

<b>STAFF USE ONLY</b>		Type of Search	Vendors and cost where applicable
Searcher:	<u>EJ</u>	NA Sequence (#)	STN <u>\$ 402.69</u>
Searcher Phone #:		AA Sequence (#)	Dialog
Searcher Location:		Structure (#)	<u>(3)</u> Questel/Orbit
Date Searcher Picked Up:		Bibliographic	<u>(400)</u> Dr. Link
Date Completed:	<u>4-10-01</u>	Litigation	Lexis/Nexis
Searcher Prep & Review Time:	<u>10</u>	Fulltext	Sequence Systems
Clerical Prep Time:		Patent Family	WWW/Internet
Online Time:	<u>125</u>	Other	Other (specify)

=> file home  
FILE 'HOME'

=> display history full 11-

	FILE 'HCA, WPIX, JAPIO'
L1	302760 SEA PCB OR PCBS OR P(W)C(W)B OR (ELEC# OR ELECTRIC? OR PRINT? OR BOARD? OR INTEGRA? OR SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) CIRCUIT? OR PRINT? (2A) BOARD? OR IC OR ICS OR I(W)C OR (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (DEVICE? OR APP## OR APPARAT?) OR VLSI?
L2	664893 SEA PCB OR PCBS OR P(W)C(W)B OR (ELEC# OR ELECTRIC? OR PRINT? OR BOARD? OR INTEGRA? OR SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) CIRCUIT? OR PRINT? (2A) BOARD? OR IC OR ICS OR I(W)C OR (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (DEVICE? OR APP## OR APPARAT?) OR VLSI?
L3	381425 SEA PCB OR PCBS OR P(W)C(W)B OR (ELEC# OR ELECTRIC? OR PRINT? OR BOARD? OR INTEGRA? OR SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) CIRCUIT? OR PRINT? (2A) BOARD? OR IC OR ICS OR I(W)C OR (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (DEVICE? OR APP## OR APPARAT?) OR VLSI?
<b>TOTAL FOR ALL FILES</b>	
L4	1349078 SEA PCB OR PCBS OR P(W) C(W) B OR (ELEC# OR ELECTRIC? OR PRINT? OR BOARD? OR INTEGRA? OR SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) CIRCUIT? OR PRINT? (2A) BOARD? OR IC OR ICS OR I(W) C OR (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (DEVICE? OR APP## OR APPARAT?) OR VLSI?
L5	18692 SEA (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (CHIP OR CHIPS OR DIE OR DIES OR WAFER? OR DISC# OR DISK? OR BLANK OR BLANKS)
L6	78807 SEA (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (CHIP OR CHIPS OR DIE OR DIES OR WAFER? OR DISC# OR DISK? OR BLANK OR BLANKS)
L7	39479 SEA (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (CHIP OR CHIPS OR DIE OR DIES OR WAFER? OR DISC# OR DISK? OR BLANK OR BLANKS)
<b>TOTAL FOR ALL FILES</b>	
L8	136978 SEA (SEMICOND? OR SEMI(A) (COND# OR CONDUCT?)) (2A) (CHIP OR CHIPS OR DIE OR DIES OR WAFER? OR DISC# OR DISK? OR BLANK OR BLANKS)
L9	823827 SEA WIRE# OR WIRING# OR HARNESS? OR LEAD OR LEADS OR BUMP# OR PAD OR PADS
L10	726027 SEA WIRE# OR WIRING# OR HARNESS? OR LEAD OR LEADS OR BUMP# OR PAD OR PADS
L11	463080 SEA WIRE# OR WIRING# OR HARNESS? OR LEAD OR LEADS OR BUMP# OR PAD OR PADS
<b>TOTAL FOR ALL FILES</b>	
L12	2012934 SEA WIRE# OR WIRING# OR HARNESS? OR LEAD OR LEADS OR BUMP# OR PAD OR PADS
L13	344563 SEA LAMIN? OR LAMEL? OR MULTILAYER? OR MULTIFILM? OR MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL

OR FEW OR MANY OR NUMEROUS OR MANIFOLD? OR MULTIFOLD? OR  
MULTITUD?) (2A) (LAYER? OR FILM? OR COAT?)

L14 301948 SEA LAMIN? OR LAMEL? OR MULTILAYER? OR MULTIFILM? OR  
MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL  
OR FEW OR MANY OR NUMEROUS OR MANIFOLD? OR MULTIFOLD? OR  
MULTITUD?) (2A) (LAYER? OR FILM? OR COAT?)

L15 237660 SEA LAMIN? OR LAMEL? OR MULTILAYER? OR MULTIFILM? OR  
MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL  
OR FEW OR MANY OR NUMEROUS OR MANIFOLD? OR MULTIFOLD? OR  
MULTITUD?) (2A) (LAYER? OR FILM? OR COAT?)

TOTAL FOR ALL FILES

L16 884171 SEA LAMIN? OR LAMEL? OR MULTILAYER? OR MULTIFILM? OR  
MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL  
OR FEW OR MANY OR NUMEROUS OR MANIFOLD? OR MULTIFOLD? OR  
MULTITUD?) (2A) (LAYER? OR FILM? OR COAT?)

L17 48614 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR INTER(2A) (LAYER?  
OR FILM? OR COAT?)

L18 19922 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR INTER(2A) (LAYER?  
OR FILM? OR COAT?)

L19 19472 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR INTER(2A) (LAYER?  
OR FILM? OR COAT?)

TOTAL FOR ALL FILES

L20 88008 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR INTER(2A) (LAYER?  
OR FILM? OR COAT?)

L21 1877 SEA DAMASCENE#

L22 1452 SEA DAMASCENE#

L23 334 SEA DAMASCENE#

TOTAL FOR ALL FILES

L24 3663 SEA DAMASCENE#

FILE 'LCA'

L25 62 SEA (CVD OR (CHEMICAL? OR CHEM) (2A) (VAPOR? OR VAPOUR?) (2A)  
DEPOSIT? OR OMCVD OR MOCVD OR LPCVD OR PECVD OR HFCVD  
OR ULPCVD OR PACVD OR PCVD)/BI,AB

FILE 'HCA, WPIX, JAPIO'

L26 94489 SEA CVD# OR (CHEMICAL? OR CHEM# OR PHYSICAL? OR PHYS#) (2A)  
(VAPOR? OR VAPOUR?) (2A) DEPOSIT? OR OMCVD OR MOCVD OR  
LPCVD OR PECVD OR HFCVD OR ULPCVD OR PACVD OR PCVD OR  
PVD

L27 30746 SEA CVD# OR (CHEMICAL? OR CHEM# OR PHYSICAL? OR PHYS#) (2A)  
(VAPOR? OR VAPOUR?) (2A) DEPOSIT? OR OMCVD OR MOCVD OR  
LPCVD OR PECVD OR HFCVD OR ULPCVD OR PACVD OR PCVD OR  
PVD

L28 26036 SEA CVD# OR (CHEMICAL? OR CHEM# OR PHYSICAL? OR PHYS#) (2A)  
(VAPOR? OR VAPOUR?) (2A) DEPOSIT? OR OMCVD OR MOCVD OR  
LPCVD OR PECVD OR HFCVD OR ULPCVD OR PACVD OR PCVD OR  
PVD

TOTAL FOR ALL FILES

L29 151271 SEA CVD# OR (CHEMICAL? OR CHEM# OR PHYSICAL? OR PHYS#) (2A)  
(VAPOR? OR VAPOUR?) (2A) DEPOSIT? OR OMCVD OR MOCVD OR  
LPCVD OR PECVD OR HFCVD OR ULPCVD OR PACVD OR PCVD OR

## PVD

L30 407684 SEA ANNEAL? OR TEMPER OR TEMPERS OR TEMPERRED OR  
TEMPERED OR TEMPERRING# OR TEMPERING# OR QUENCH?

L31 78339 SEA ANNEAL? OR TEMPER OR TEMPERS OR TEMPERRED OR  
TEMPERED OR TEMPERRING# OR TEMPERING# OR QUENCH?

L32 44675 SEA ANNEAL? OR TEMPER OR TEMPERS OR TEMPERRED OR  
TEMPERED OR TEMPERRING# OR TEMPERING# OR QUENCH?

## TOTAL FOR ALL FILES

L33 530698 SEA ANNEAL? OR TEMPER OR TEMPERS OR TEMPERRED OR  
TEMPERED OR TEMPERRING# OR TEMPERING# OR QUENCH?

L34 346414 SEA POLISH? OR CMP OR C(W)M(W)P OR FURBISH? OR BURNISH?  
OR SMOOTH? OR PLANAR?

L35 312986 SEA POLISH? OR CMP OR C(W)M(W)P OR FURBISH? OR BURNISH?  
OR SMOOTH? OR PLANAR?

L36 203296 SEA POLISH? OR CMP OR C(W)M(W)P OR FURBISH? OR BURNISH?  
OR SMOOTH? OR PLANAR?

## TOTAL FOR ALL FILES

L37 862696 SEA POLISH? OR CMP OR C(W) M(W) P OR FURBISH? OR  
BURNISH? OR SMOOTH? OR PLANAR?

## FILE 'LCA'

L38 14808 SEA (INHIBIT? OR HINDER? OR IMPED? OR ARREST? OR REDUC?  
OR REDN# OR RESIST? OR SUPPRESS? OR RETARD? OR PROHIBIT?  
OR PREVENT? OR BLOCK? OR ELIMINAT? /BI,AB

## FILE 'HCA, WPIX, JAPIO'

L39 46271 SEA (INHIBIT? OR HINDER? OR IMPED? OR ARREST? OR REDUC?  
OR REDN# OR RESIST? OR SUPPRESS? OR RETARD? OR PROHIBIT?  
OR PREVENT? OR BLOCK? OR ELIMINAT? OR LOW OR LOWER? OR  
LESS? OR DIMINISH? OR DECREAS? OR BARRIER?) (2A) DIFFUS?

L40 16369 SEA (INHIBIT? OR HINDER? OR IMPED? OR ARREST? OR REDUC?  
OR REDN# OR RESIST? OR SUPPRESS? OR RETARD? OR PROHIBIT?  
OR PREVENT? OR BLOCK? OR ELIMINAT? OR LOW OR LOWER? OR  
LESS? OR DIMINISH? OR DECREAS? OR BARRIER?) (2A) DIFFUS?

L41 11485 SEA (INHIBIT? OR HINDER? OR IMPED? OR ARREST? OR REDUC?  
OR REDN# OR RESIST? OR SUPPRESS? OR RETARD? OR PROHIBIT?  
OR PREVENT? OR BLOCK? OR ELIMINAT? OR LOW OR LOWER? OR  
LESS? OR DIMINISH? OR DECREAS? OR BARRIER?) (2A) DIFFUS?

## TOTAL FOR ALL FILES

L42 74125 SEA (INHIBIT? OR HINDER? OR IMPED? OR ARREST? OR REDUC?  
OR REDN# OR RESIST? OR SUPPRESS? OR RETARD? OR PROHIBIT?  
OR PREVENT? OR BLOCK? OR ELIMINAT? OR LOW OR LOWER? OR  
LESS? OR DIMINISH? OR DECREAS? OR BARRIER?) (2A) DIFFUS?

## FILE 'REGISTRY'

L43 313 SEA (TI(L)N)/ELS (L) 2/ELC.SUB  
E TANTALUM/CN

L44 1 SEA TANTALUM/CN

L45 140 SEA (TA(L)N)/ELS (L) 2/ELC.SUB

L46 93 SEA (W(L)N)/ELS (L) 2/ELC.SUB

L47 587 SEA ((TI OR TA)(L)(AL OR SI)(L)N)/ELS (L) 3/ELC.SUB  
E IODINE/CN

L48            1 SEA IODINE/CN  
L49            430 SEA (C(L)(H OR D)(L)I)/ELS (L) 3/ELC.SUB AND 1-3/C

FILE 'HCA, WPIX, JAPIO'  
L50        139350 SEA TA OR TANTALUM# OR WN OR TIALN OR ALTIN OR TISIN OR  
            SITIN OR TASIN OR SITAN OR (TITANIUM# OR TI OR TANTALUM#  
            OR TA OR TUNGSTEN#) (A) NITRIDE#  
L51        40618 SEA TA OR TANTALUM# OR WN OR TIALN OR ALTIN OR TISIN OR  
            SITIN OR TASIN OR SITAN OR (TITANIUM# OR TI OR TANTALUM#  
            OR TA OR TUNGSTEN#) (A) NITRIDE#  
L52        24828 SEA TA OR TANTALUM# OR WN OR TIALN OR ALTIN OR TISIN OR  
            SITIN OR TASIN OR SITAN OR (TITANIUM# OR TI OR TANTALUM#  
            OR TA OR TUNGSTEN#) (A) NITRIDE#  
TOTAL FOR ALL FILES  
L53        204796 SEA TA OR TANTALUM# OR WN OR TIALN OR ALTIN OR TISIN OR  
            SITIN OR TASIN OR SITAN OR (TITANIUM# OR TI OR TANTALUM#  
            OR TA OR TUNGSTEN#) (A) NITRIDE#  
L54        70954 SEA (L43 OR L44 OR L45 OR L46 OR L47)  
L55            1 SEA (L43 OR L44 OR L45 OR L46 OR L47)  
L56            0 SEA (L43 OR L44 OR L45 OR L46 OR L47)  
TOTAL FOR ALL FILES  
L57        70955 SEA (L43 OR L44 OR L45 OR L46 OR L47)  
L58        289853 SEA L48 OR IODINE# OR IODAT? OR IODINAT? OR IODIDE# OR  
            I2  
L59        34160 SEA L48 OR IODINE# OR IODAT? OR IODINAT? OR IODIDE# OR  
            I2  
L60        11882 SEA L48 OR IODINE# OR IODAT? OR IODINAT? OR IODIDE# OR  
            I2  
TOTAL FOR ALL FILES  
L61        335895 SEA L48 OR IODINE# OR IODAT? OR IODINAT? OR IODIDE# OR  
            I2  
L62        29698 SEA L49 OR CH3I OR C2H5I OR CH3CH2I OR CD3I OR ICD3 OR  
            ICH3 OR CH2I2 OR I2CH2 OR DIIODOMETHANE# OR METHYLENE# (A)  
            (IODIDE# OR DIIODIDE#)  
L63        402 SEA L49 OR CH3I OR C2H5I OR CH3CH2I OR CD3I OR ICD3 OR  
            ICH3 OR CH2I2 OR I2CH2 OR DIIODOMETHANE# OR METHYLENE# (A)  
            (IODIDE# OR DIIODIDE#)  
L64        54 SEA L49 OR CH3I OR C2H5I OR CH3CH2I OR CD3I OR ICD3 OR  
            ICH3 OR CH2I2 OR I2CH2 OR DIIODOMETHANE# OR METHYLENE# (A)  
            (IODIDE# OR DIIODIDE#)  
TOTAL FOR ALL FILES  
L65        30154 SEA L49 OR CH3I OR C2H5I OR CH3CH2I OR CD3I OR ICD3 OR  
            ICH3 OR CH2I2 OR I2CH2 OR DIIODOMETHANE# OR METHYLENE# (A)  
            (IODIDE# OR DIIODIDE#)

FILE 'LCA'  
L66        7645 SEA (FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR  
            OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR LEAF? OR  
            FOIL? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR  
            SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR  
            OVERSPREAD?) /BI,AB

FILE 'HCA, WPIX, JAPIO'

L67 4040 SEA (ENHANCER? OR ENHANCING# OR ENHANCEMENT?) (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

L68 1481 SEA (ENHANCER? OR ENHANCING# OR ENHANCEMENT?) (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

L69 1031 SEA (ENHANCER? OR ENHANCING# OR ENHANCEMENT?) (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

TOTAL FOR ALL FILES

L70 6552 SEA (ENHANCER? OR ENHANCING# OR ENHANCEMENT?) (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

L71 17047 SEA ENHANC? (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

L72 8775 SEA ENHANC? (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

L73 5485 SEA ENHANC? (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

TOTAL FOR ALL FILES

L74 31307 SEA ENHANC? (2A) (CHEMICAL? OR CHEM# OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?)

L75 867 SEA (L1 OR L5) AND L9 AND L39

L76 855 SEA (L2 OR L6) AND L10 AND L40

L77 1082 SEA (L3 OR L7) AND L11 AND L41

TOTAL FOR ALL FILES

L78 2804 SEA (L4 OR L8) AND L12 AND L42

L79 15427 SEA L39 (3A) (FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?) OR

L80            7064 DIFFUS? (2A) BARRIER?  
 SEA L40 (3A) (FILM? OR THIN FILM? OR LAYER? OR OVERLAY? OR  
 OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR  
 TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR  
 ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?) OR  
 DIFFUS? (2A) BARRIER?

L81            3867 SEA L41 (3A) (FILM? OR THIN FILM? OR LAYER? OR OVERLAY? OR  
 OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR  
 TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR  
 ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?) OR  
 DIFFUS? (2A) BARRIER?

TOTAL FOR ALL FILES

L82            26358 SEA L42 (3A) (FILM? OR THIN FILM? OR LAYER? OR OVERLAY? OR  
 OVERLAID? OR LAMIN? OR LAMEL? OR SHEET? OR COAT? OR  
 TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR COVER? OR  
 ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD?) OR  
 DIFFUS? (2A) BARRIER?

L83            701 SEA L75 AND L79

L84            578 SEA L76 AND L80

L85            563 SEA L77 AND L81

TOTAL FOR ALL FILES

L86            1842 SEA L78 AND L82

L87            38 SEA L83 AND L21

L88            35 SEA L84 AND L22

L89            3 SEA L85 AND L23

TOTAL FOR ALL FILES

L90            76 SEA L86 AND L24

L91            30 SEA L87 AND (L13 OR L30 OR L26 OR L30 OR L34)

L92            28 SEA L88 AND (L14 OR L30 OR L27 OR L31 OR L35)

L93            3 SEA L89 AND (L15 OR L30 OR L28 OR L32 OR L36)

TOTAL FOR ALL FILES

L94            61 SEA L90 AND (L16 OR L30 OR L29 OR L33 OR L37)

L95            15 SEA L87 AND (L50 OR L54)

L96            16 SEA L88 AND (L51 OR L55)

L97            0 SEA L89 AND (L52 OR L56)

TOTAL FOR ALL FILES

L98            31 SEA L90 AND (L53 OR L57)

L99            2311 SEA (L1 OR L5) AND L9 AND (L50 OR L54)

L100          1527 SEA (L2 OR L6) AND L10 AND (L51 OR L55)

L101          991 SEA (L3 OR L7) AND L11 AND (L52 OR L56)

TOTAL FOR ALL FILES

L102          4829 SEA (L4 OR L8) AND L12 AND (L53 OR L57)

L103          54 SEA L99 AND L21

L104          56 SEA L100 AND L22

L105          7 SEA L101 AND L23

TOTAL FOR ALL FILES

L106          117 SEA L102 AND L24

L107          10 SEA L103 AND L17

L108          10 SEA L104 AND L18

L109          5 SEA L105 AND L19

TOTAL FOR ALL FILES

L110          25 SEA L106 AND L20

L111            7 SEA L103 AND L13  
L112            7 SEA L104 AND L14  
L113            1 SEA L105 AND L15  
TOTAL FOR ALL FILES  
L114            15 SEA L106 AND L16  
L115            19 SEA L103 AND L26  
L116            22 SEA L104 AND L27  
L117            2 SEA L105 AND L28  
TOTAL FOR ALL FILES  
L118            43 SEA L106 AND L29  
L119            8 SEA L103 AND L30  
L120            11 SEA L104 AND L31  
L121            0 SEA L105 AND L32  
TOTAL FOR ALL FILES  
L122            19 SEA L106 AND L33  
L123            29 SEA L103 AND L34  
L124            34 SEA L104 AND L35  
L125            5 SEA L105 AND L36  
TOTAL FOR ALL FILES  
L126            68 SEA L106 AND L37  
L127            14 SEA L115 AND L123  
L128            17 SEA L116 AND L124  
L129            1 SEA L117 AND L125  
TOTAL FOR ALL FILES  
L130            32 SEA L118 AND L126  
L131            31 SEA (L1 OR L5) AND L9 AND L67  
L132            49 SEA (L2 OR L6) AND L10 AND L68  
L133            48 SEA (L3 OR L7) AND L11 AND L69  
TOTAL FOR ALL FILES  
L134            128 SEA (L4 OR L8) AND L12 AND L70  
L135            4 SEA L131 AND (L58 OR L62)  
L136            8 SEA L132 AND (L59 OR L63)  
L137            0 SEA L133 AND (L60 OR L64)  
TOTAL FOR ALL FILES  
L138            12 SEA L134 AND (L61 OR L65)  
L139            114 SEA (L1 OR L5) AND L9 AND L71  
L140            269 SEA (L2 OR L6) AND L10 AND L72  
L141            259 SEA (L3 OR L7) AND L11 AND L73  
TOTAL FOR ALL FILES  
L142            642 SEA (L4 OR L8) AND L12 AND L74  
L143            4 SEA L139 AND (L58 OR L62)  
L144            9 SEA L140 AND (L59 OR L63)  
L145            0 SEA L141 AND (L60 OR L64)  
TOTAL FOR ALL FILES  
L146            13 SEA L142 AND (L61 OR L65)  
L147            4 SEA L139 AND L21  
L148            14 SEA L140 AND L22  
L149            1 SEA L141 AND L23  
TOTAL FOR ALL FILES  
L150            19 SEA L142 AND L24  
L151            166 SEA (L1 OR L5) AND L9 AND L58  
L152            154 SEA (L2 OR L6) AND L10 AND L59

L153 62 SEA (L3 OR L7) AND L11 AND L60  
TOTAL FOR ALL FILES  
L154 382 SEA (L4 OR L8) AND L12 AND L61  
L155 11 SEA (L1 OR L5) AND L9 AND L62  
L156 3 SEA (L2 OR L6) AND L10 AND L63  
L157 0 SEA (L3 OR L7) AND L11 AND L64  
TOTAL FOR ALL FILES  
L158 14 SEA (L4 OR L8) AND L12 AND L65  
L159 6 SEA L151 AND L21  
L160 8 SEA L152 AND L22  
L161 0 SEA L153 AND L23  
TOTAL FOR ALL FILES  
L162 14 SEA L154 AND L24  
L163 43 SEA (L1 OR L5) AND L9 AND (L39 OR L50 OR L54) AND (L71  
OR L58 OR L62)  
L164 59 SEA (L2 OR L6) AND L10 AND (L40 OR L51 OR L55) AND (L72  
OR L59 OR L63)  
L165 19 SEA (L3 OR L7) AND L11 AND (L41 OR L52 OR L56) AND (L73  
OR L60 OR L64)  
TOTAL FOR ALL FILES  
L166 121 SEA (L4 OR L8) AND L12 AND (L42 OR L53 OR L57) AND (L74  
OR L61 OR L65)  
L167 5 SEA L163 AND L21  
L168 12 SEA L164 AND L22  
L169 0 SEA L165 AND L23  
TOTAL FOR ALL FILES  
L170 17 SEA L166 AND L24  
L171 5 SEA L163 AND L17  
L172 17 SEA L164 AND L18  
L173 4 SEA L165 AND L19  
TOTAL FOR ALL FILES  
L174 26 SEA L166 AND L20  
L175 5 SEA L163 AND L13  
L176 9 SEA L164 AND L14  
L177 1 SEA L165 AND L15  
TOTAL FOR ALL FILES  
L178 15 SEA L166 AND L16  
L179 11 SEA L163 AND L26  
L180 31 SEA L164 AND L27  
L181 2 SEA L165 AND L28  
TOTAL FOR ALL FILES  
L182 44 SEA L166 AND L29  
L183 6 SEA L163 AND L30  
L184 8 SEA L164 AND L31  
L185 2 SEA L165 AND L32  
TOTAL FOR ALL FILES  
L186 16 SEA L166 AND L33  
L187 11 SEA L163 AND L34  
L188 21 SEA L164 AND L35  
L189 1 SEA L165 AND L36  
TOTAL FOR ALL FILES  
L190 33 SEA L166 AND L37

L191 5 SEA L179 AND L187  
L192 15 SEA L180 AND L188  
L193 1 SEA L181 AND L189  
TOTAL FOR ALL FILES  
L194 21 SEA L182 AND L190

FILE 'JAPIO'  
L195 18 SEA L89 OR L93 OR L109 OR L113 OR L117 OR L125 OR L129  
OR L173 OR L177 OR L181 OR L185 OR L189 OR L193

FILE 'HCA'  
L196 8 SEA L167 OR L171  
L197 25 SEA (L111 OR L119 OR L135 OR L143 OR L147 OR L159 OR  
L175 OR L183 OR L191) NOT L196  
L198 25 SEA (L95 OR L107 OR L127 OR L155) NOT (L196 OR L197)  
L199 18 SEA L91 NOT (L196 OR L197 OR L198)

FILE 'WPIX'  
L200 22 SEA L168 OR L172  
L201 22 SEA (L112 OR L136 OR L144 OR L156 OR L160 OR L176 OR  
L184) NOT L200  
L202 21 SEA (L96 OR L108 OR L120 OR L128 OR L148 OR L192) NOT  
(L200 OR L201)  
L203 12 SEA L92 NOT (L200 OR L201 OR L202)

FILE 'JAPIO'  
L204 8 SEA L195 AND 1900-1999/PY

FILE 'WPIX'  
L205 5 SEA L200 AND 1900-1999/PY  
L206 7 SEA L201 AND 1900-1999/PY  
L207 4 SEA L202 AND 1900-1999/PY  
L208 0 SEA L203 AND 1900-1999/PY

FILE 'HCA'  
L209 0 SEA L196 AND 1907-1999/PY  
L210 6 SEA L197 AND 1907-1999/PY  
L211 10 SEA L198 AND 1907-1999/PY  
L212 0 SEA L199 AND 1907-1999/PY

FILE 'HCA, WPIX, JAPIO'  
L213 61291 SEA (METAL#### OR COPPER# OR CU) (2A) (WIRE# OR WIRING# OR  
HARNESS? OR FILAMENT? OR STRAND? OR RIBBON? OR LEAD OR  
LEADS OR PAD OR PADS OR BUMP#)  
L214 50127 SEA (METAL#### OR COPPER# OR CU) (2A) (WIRE# OR WIRING# OR  
HARNESS? OR FILAMENT? OR STRAND? OR RIBBON? OR LEAD OR  
LEADS OR PAD OR PADS OR BUMP#)  
L215 30411 SEA (METAL#### OR COPPER# OR CU) (2A) (WIRE# OR WIRING# OR  
HARNESS? OR FILAMENT? OR STRAND? OR RIBBON? OR LEAD OR  
LEADS OR PAD OR PADS OR BUMP#)

TOTAL FOR ALL FILES  
L216 141829 SEA (METAL#### OR COPPER# OR CU) (2A) (WIRE# OR WIRING# OR

HARNESS? OR FILAMENT? OR STRAND? OR RIBBON? OR LEAD OR  
LEADS OR PAD OR PADS OR BUMP#)

L217 13 SEA (L1 OR L5) AND L213 AND (L39 OR L50 OR L54) AND (L71  
OR L58 OR L62)  
L218 23 SEA (L2 OR L6) AND L214 AND (L40 OR L51 OR L55) AND (L72  
OR L59 OR L63)  
L219 7 SEA (L3 OR L7) AND L215 AND (L41 OR L52 OR L56) AND (L73  
OR L60 OR L64)  
TOTAL FOR ALL FILES  
L220 43 SEA (L4 OR L8) AND L216 AND (L42 OR L53 OR L57) AND (L74  
OR L61 OR L65)

## FILE 'HCA'

L221 12 SEA L217 NOT (L210 OR L211)  
L222 2 SEA L221 AND 1907-1999/PY

## FILE 'WPIX'

L223 22 SEA L218 NOT (L205 OR L206 OR L207)  
L224 2 SEA L223 AND 1900-1999/PY

## FILE 'JAPIO'

L225 5 SEA L219 NOT L204  
L226 3 SEA L225 AND 1900-1999/PY

=> file japios  
FILE 'JAPIO'  
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FILE LAST UPDATED: 4 APR 2003 <20030404/UP>  
FILE COVERS APR 1973 TO NOVEMBER 29, 2002

=> d 1204 1-8 ibib abs ind

L204 ANSWER 1 OF 8 JAPIO COPYRIGHT 2003 JPO  
ACCESSION NUMBER: 1999-340226 JAPIO  
TITLE: MANUFACTURE OF SEMICONDUCTOR  
DEVICE  
INVENTOR: IKEDA SATOSHI  
PATENT ASSIGNEE(S): SONY CORP  
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 11340226	A	19991210	Heisei	H01L021-3205

## APPLICATION INFORMATION

STN FORMAT:	JP 1998-141154	19980522
ORIGINAL:	JP10141154	Heisei
PRIORITY APPLN. INFO.:	JP 1998-141154	19980522
SOURCE:	PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined	

## Applications, Vol. 1999

AN 1999-340226 JAPIO  
 AB PROBLEM TO BE SOLVED: To provide a method for manufacturing a semiconductor device, which is capable of preventing the generation of dishing of a conductive film, such as a Cu film embedded in a recess like a **wiring** groove and also effectively preventing the diffusion of constituent elements of the conductive film embedded in the recess, when the conductive film is embedded through an anti-diffusion film in the recess with the use of a **polishing** technique, such as **CMP** method.  
 SOLUTION: Connection holes 8 and **wiring** groove 9 are made in an **interlayer** insulating film 7 on a semiconductor substrate 1, and thereafter a Ta film 10 as a first anti-diffusion film is formed over the entire surface of the substrate by a sputtering method or the like. Next, the Ta film 10 is **polished** by the **CMP** method to be left only in the interiors of the connection holes and **wiring** grooves 9. Subsequently, a TiN film 11 as a second anti-diffusion film is formed on the entire surface of the substrate by the sputtering method or the like, and a Cu film for **wiring** formation is formed as sufficiently thick on the TiN film by an electroplating or the like to be completely filled in the connection holes 8 and **wiring** grooves 9. Next, the Cu film and TiN film 11 is **polished** by the **CMP** method to be left only in the interiors of the connection holes 8 and **wiring** grooves 9, thereby forming a Cu **wiring** 14 as a dual **damascene wiring**.

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 IC, ICM H01L021-3205

L204 ANSWER 2 OF 8 JAPIO COPYRIGHT 2003 JPO  
 ACCESSION NUMBER: 1998-189592 JAPIO  
 TITLE: MANUFACTURING METHOD OF SEMICONDUCTOR  
 DEVICE  
 INVENTOR: MIYAMOTO YASUSHI  
 PATENT ASSIGNEE(S): NIPPON STEEL CORP  
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 10189592	A	19980721	Heisei	H01L021-3205

X

## APPLICATION INFORMATION

STN FORMAT:	JP 1996-355964	19961225
ORIGINAL:	JP08355964	Heisei
PRIORITY APPLN. INFO.:	JP 1996-355964	19961225
SOURCE:	PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998	

AN 1998-189592 JAPIO  
 AB PROBLEM TO BE SOLVED: To restrain a buried Cu **wiring** provided through a **damascene** method from increasing in **interlayer** capacitance due to a barrier film provided so as

to prevent Cu from diffusing into an **interlayer** insulating film.

SOLUTION: A **titanium nitride** film 1 is formed so as to cover the inner surface of a ditch DT provided to an **interlayer** insulating film 3, a Cu film 2 is formed thereon, and the Cu film 2 and the **titanium nitride** 1 are all removed from the surface of the insulating film 3 except the ditch DT through a chemical mechanical polish(CMP) method. A **titanium tungsten nitride** film 4 is formed on the surface of the Cu film 2 recessed by a **CMP** method in the ditch DT, and the **titanium tungsten nitride** film 4 is left unremoved only on the recessed surface of the Cu film in the ditch DT through a resist etch-back method.

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IC ICM H01L021-3205

L204 ANSWER 3 OF 8 JAPIO COPYRIGHT 2003 JPO

ACCESSION NUMBER: 1996-078525 JAPIO

TITLE: SEMICONDUCTOR DEVICE AND  
FABRICATION THEREOF

INVENTOR: KATO YOSHIHIKO

PATENT ASSIGNEE(S): SEIKO EPSON CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 08078525	A	<u>19960322</u>	Heisei	H01L021-768

#### APPLICATION INFORMATION

STN FORMAT: JP 1994-213995 19940907

ORIGINAL: JP06213995 Heisei

PRIORITY APPLN. INFO.: JP 1994-213995 19940907  
X SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996

AN 1996-078525 JAPIO

AB PURPOSE: To enhance the long term reliability at a **wiring** part by forming a **wiring** through sputtering and then depositing a metal at a part in a contact hole not covered well with a **wiring** metal by electrolytic plating or electroless plating using the **wiring** itself as a cathode thereby improving the step coverage.

CONSTITUTION: A metal **wiring** 108 comprises a first layer, i.e., a barrier metal layer of titanium and **titanium nitride** for preventing silicification reaction between a semiconductor substrate and a **wiring** material such as aluminum, and a second layer of aluminum alloy containing silicon or copper formed by sputtering. A low coverage part 109 in a contact hole 107 is then buried in a metal plating **layer** 110 thus enhancing reliability of the **wiring** layer in a **semiconductor device**. Furthermore insulation of an **interlayer** insulation film, deposited above a contact hole,

can be prevented from deteriorating.

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IC ICM H01L021-768

ICS H01L021-288

L204 ANSWER 4 OF 8 JAPIO COPYRIGHT 2003 JPO

ACCESSION NUMBER: 1995-078789 JAPIO

TITLE: MANUFATURE OF SEMICONDUCTOR

**DEVICE**

INVENTOR: HAYASHI JUN; NAKAJIMA JUNICHIRO; IKEDA KAZUKO;

AIZAWA KAZUO

PATENT ASSIGNEE(S) : NEC CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 07078789	A	19950320	Heisei	H01L021-28

**APPLICATION INFORMATION**

STN FORMAT: JP 1993-222960 19930908

ORIGINAL: JP05222960 Heisei

PRIORITY APPLN. INFO.: JP 1993-222960 19930908

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995

AN 1995-078789 JAPIO

AB PURPOSE: To obtain a **semiconductor device** wherein an upper **wiring** layer on which bonding **pads** are provided and an **interlayer** insulating film that serves as a ground for the upper **wiring** layer can be **enhanced** in adhesion and lessened in contact resistance between them.

CONSTITUTION: After an N<SP>+</SP>-type diffusion, layer 103 or the like is formed to serve as a lower **wiring** layer, an **interlayer** insulating film 105 of silicon oxide is formed by a plasma CVD method using mixed material gas of silane gas and N<SB>2</SB>O gas. A contact hole 106 is formed, and then a titanium film 107 and a **titanium nitride** film 108 are formed and a titanium silicide film 109 is formed on the base of the contact hole 106 through an RTA process carried out under prescribed conditions. At least, an aluminum alloy film 110 is formed and then an upper **wiring** layer of at least three-layered structure is formed through a prescribed patterning process.

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IC ICM H01L021-28

ICS H01L021-316; H01L021-3205

L204 ANSWER 5 OF 8 JAPIO COPYRIGHT 2003 JPO

ACCESSION NUMBER: 1992-179148 JAPIO

TITLE: SEMICONDUCTOR DEVICE AND

MANUFACTURE THEREOF

INVENTOR: KANAZAWA MASATO

PATENT ASSIGNEE(S) : MATSUSHITA ELECTRON CORP  
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 04179148	A	19920625	Heisei	H01L021-90

## APPLICATION INFORMATION

STN FORMAT: JP 1990-304357 19901108  
 ORIGINAL: JP02304357 Heisei  
 PRIORITY APPLN. INFO.: JP 1990-304357 19901108  
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992

AN 1992-179148 JAPIO

AB PURPOSE: To enhance an aluminum alloy layer in coverage rate at a contact opening by a method wherein non-conductive polycrystalline silicon or silicon oxide is filled into only the contact opening through the intermediary of a metal compound layer composed of a titanium layer and a **titanium nitride** layer.

CONSTITUTION: A field insulating film 12 is formed on a P-type semiconductor substrate 11, furthermore an N-type diffusion layer 15 is formed, and a contact opening 14 is formed thereon through the intermediary of an **interlayer** insulating film 13. Then, the contact opening 4 is cleaned, a titanium layer and a **titanium nitride** layer are deposited in succession to form a metal compound layer 16. Furthermore, a polycrystalline silicon layer 17 is deposited thereon. Moreover, the polycrystalline silicon layer 17 other than its part formed in the contact opening is removed through a dry etching method which is high in selection ratio to the base metal compound layer. Then, an aluminum alloy layer is deposited thereon to form an upper **wiring** layer.

By this setup, an aluminum or an aluminum alloy layer serving as an upper **wiring** can be **enhanced in coverage** rate at the step of a contact opening.

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IC ICM .H01L021-90

ICS H01L021-285; H01L021-3205

L204 ANSWER 6 OF 8 JAPIO COPYRIGHT 2003 JPO

ACCESSION NUMBER: 1991-177027 JAPIO

TITLE: SEMICONDUCTOR DEVICE AND  
MANUFACTURE THEREOF

INVENTOR: SHIMIZU MASAHIRO; KUROI TAKASHI

PATENT ASSIGNEE(S) : MITSUBISHI ELECTRIC CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 03177027	A	19910801	Heisei	H01L021-336

## APPLICATION INFORMATION

STN FORMAT: JP 1989-317280 19891205

ORIGINAL: JP01317280 Heisei  
 PRIORITY APPLN. INFO.: JP 1989-317280 19891205  
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1991

AN 1991-177027 JAPIO  
 AB PURPOSE: To enhance a gate breakdown strength by forming a titanium silicide film, and then implanting nitrogen ions or oxygen ions into a polysilicon to form an SiNx or SiOy layer.  
 CONSTITUTION: A titanium silicide film 7 is formed only on a gate polysilicon, source/drain regions of a self-aligned silicide transistor. Then, after nitrogen ions are implanted, an interlayer insulating film 8 is formed. Thereafter, a heat treatment for reflowing is executed, the implanted nitrogen and a gate polysilicon 8 or a substrate silicon 1 are reacted to form an SiNx film 11. Thereafter, after a contact hole 9 is opened, metal wirings 10 of aluminum, etc., are formed. Thus, the SiNx is formed on the gate polysilicon to suppress diffusion of titanium to eliminate deterioration of a gate insulating film, thereby enhancing a gate breakdown strength.  
 COPYRIGHT: (C)1991,JPO&Japio  
 IC ICM H01L021-336  
 ICS H01L029-784

L204 ANSWER 7 OF 8 JAPIO COPYRIGHT 2003 JPO  
 ACCESSION NUMBER: 1989-264239 JAPIO  
 TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE  
 INVENTOR: SUDO ITSUKI; KURE TOKUO; NISHIDA TAKASHI; KADOTA SHINICHIRO  
 PATENT ASSIGNEE(S): HITACHI LTD  
 PATENT INFORMATION:

PATENT NO.	KIND	DATE	ERA	MAIN IPC
JP 01264239	A	19891020	Heisei	H01L021-88

## APPLICATION INFORMATION

STN FORMAT: JP 1988-91549 19880415  
 ORIGINAL: JP63091549 Showa  
 PRIORITY APPLN. INFO.: JP 1988-91549 19880415  
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989

AN 1989-264239 JAPIO  
 AB PURPOSE: To form a multilayer-film wiring layer of high reliability by a method wherein a first Al film which has been used as a mask is left as it is and a barrier metal layer and a second Al film are formed one after another on it.  
 CONSTITUTION: An insulating film 102 is formed on an Si substrate 101; a first Al film 103 is formed on it. Then, an opening part is formed in the first Al film 103; the insulating film 102 is dry-etched by making use of the Al film 103 as a mask; a contact

hole 104 is made. Then, a TiN film, a Ti film, a Ta film or a W film is formed as a barrier metal layer 105. After that, a second Al film 106 is formed; a **wiring** layer of a three-layer film is formed in a part other than a two-layer film composed of the barrier metal layer 105 and the second Al layer 106 which cover the contact hole 104. Accordingly, Si is not precipitated in the second Al film 106; it is possible to prevent an increase in a contact resistance; it is possible to prevent a disconnection due to electromigration; the reliability of the **wiring layer** can be **enhanced**.

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IC ICM H01L021-88

ICS H01L021-28; H01L021-90

L204 ANSWER 8 OF 8 JAPIO COPYRIGHT 2003 JPO

ACCESSION NUMBER: 1986-187232 JAPIO

TITLE: MANUFACTURE OF SEMICONDUCTOR

**DEVICE**

INVENTOR: FUJITA ICHIRO; YAGIMURA HIDEYUKI; TSUNODA KAZUO

PATENT ASSIGNEE(S): FUJITSU LTD

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 61187232	A	19860820	Showa	H01L021-28

APPLICATION INFORMATION

STN FORMAT: JP 1985-27004 19850214

ORIGINAL: JP60027004 Showa

PRIORITY APPLN. INFO.: JP 1985-27004 19850214

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1986

AN 1986-187232 JAPIO

AB PURPOSE: To inhibit the break-down failure of a contact window by forming a **titanium nitride** pattern centering on the contact window on the Al **wiring** pattern and applying a short-period flash **annealing** with a halogen lamp.

CONSTITUTION: After a contact window 15 has been formed by dry etching in an insulator layer 14 provided on a semiconductor substrate, the whole surface of the substrate is covered with Al by the electron beam evaporation method and the Al layer is photoetched to produce an Al **wiring** pattern 16. Next, a TiN film is formed on the whole surface of the pattern 16 by sputtering Ti in an atmosphere composed of Ar containing 30% of N<SB>2</SB>. The black TiN film thus obtained is patterned and subjected to plasma etching to obtain a TiN film 47 only on the Al **wiring** pattern surrounding the contact window 15. In this state, the Al **wiring** pattern is flattened to **enhance** the

coverage ratio up to 40% by applying **flash-annealing** at 1,000°C, during about 5sec using a halogen lamp.

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IC ICM H01L021-28

=> d 1226 1-3 ibib abs ind

L226 ANSWER 1 OF 3 JAPIO COPYRIGHT 2003 JPO  
 ACCESSION NUMBER: 1993-094985 JAPIO  
 TITLE: MANUFACTURE OF SEMICONDUCTOR  
 DEVICE  
 INVENTOR: YORIKANE MASAHIRO  
 PATENT ASSIGNEE(S): NEC CORP  
 PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 05094985	A	19930416	Heisei	H01L021-3205

#### APPLICATION INFORMATION

STN FORMAT: JP 1991-254027 19911002  
 ORIGINAL: JP03254027 Heisei  
 PRIORITY APPLN. INFO.: JP 1991-254027 19911002  
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1993

AN 1993-094985 JAPIO

AB PURPOSE: To enable a reattached film to be enhanced in adhesive strength by a method wherein a metal film excellent in adhesion is provided between the side face of a wiring metal film and a metal film attached gain to the side face concerned through sputtering etching.

CONSTITUTION: An opening is selectively provided to an oxide film 12 formed on a silicon substrate 11, a diffusion barrier and adhesion tungsten titanate film 13, a plating gold wire 14, and an adhesion titanium film 15 are laid thereon. In succession, a photoresist film 16 is formed, then a wiring forming region is etched, and then the titanium film 15 is removed by etching. Then, an electroplating treatment is executed, and the gold wire 14 is coated with a wiring gold plating film 17. Then, the photoresist 16 is removed, and then the titanium film 15, the gold film 14, and the tungsten titanate film 13 are removed by an etching treatment primarily composed of sputtering etching. At this point, a reattached film 18 is formed concurrently. The reattached film 18 concerned is composed of a titanium film 19 reattached to the gold plating film 17, a reattached gold film 20, and a tungsten titanate film 21.

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IC ICM H01L021-3205

ICA H01L021-28

L226 ANSWER 2 OF 3 JAPIO COPYRIGHT 2003 JPO  
 ACCESSION NUMBER: 1992-180227 JAPIO  
 TITLE: SEMICONDUCTOR DEVICE  
 INVENTOR: ISHIDA MASAYA  
 PATENT ASSIGNEE(S): TOSHIBA CORP

## PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 04180227	A	19920626	Heisei	H01L021-3205

## APPLICATION INFORMATION

STN FORMAT: JP 1990-307022 19901115  
 ORIGINAL: JP02307022 Heisei  
 PRIORITY APPLN. INFO.: JP 1990-307022 19901115  
 SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992

AN 1992-180227 JAPIO

AB PURPOSE: To enhance the close contact property of **metal wiring** with an insulating film at its substratum by a method wherein a silicon layer which is bonded, in a plurality of places, to a high-melting-point metal under the **metal wiring** and which is isolated from other wiring is provided under the insulating film under a pad part of the metal interconnection.

CONSTITUTION: A barrier metal composed of a high-melting-point metal such as W, Ti, Mo, Ta, Pt, TiW or the like is deposited, by a sputtering operation, on a layer insulating film 6 including the inside of contact holes; it is heated in a N<SB>2</SB> atmosphere; the barrier metal is reacted with polysilicon coming into contact with the metal; and it is changed to a silicon to form contact parts 11. In succession, an aluminum film is deposited by a sputtering operation; wiring is patterned by an anisotropic etching operation; and a barrier metal layer 4 and aluminum wiring 1, 3 are formed. Thereby, the close contact property of the **metal wiring** with the substratum insulating film is enhanced.

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IC ICM H01L021-3205

L226 ANSWER 3 OF 3 JAPIO COPYRIGHT 2003 JPO

ACCESSION NUMBER: 1990-283063 JAPIO

TITLE:  
**SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING**

**COMPLEMENTARY MOS CIRCUIT**  
 INVENTOR: KANO YASUO

PATENT ASSIGNEE(S): FUJI ELECTRIC CO LTD

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 02283063	A	19901120	Heisei	H01L027-092

## APPLICATION INFORMATION

STN FORMAT: JP 1989-105230 19890425  
 ORIGINAL: JP01105230 Heisei  
 PRIORITY APPLN. INFO.: JP 1989-105230 19890425

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1990

AN 1990-283063 JAPIO

AB PURPOSE: To alleviate an electric field concentration, to enhance the breakdown voltage resistance of a wiring film and to increase a current capacity by rounding the end shape of **metal wirings** in conductive contact with a **diffused layer resistor** of an input side, and removing a metal edge.

CONSTITUTION: The ends of aluminum wirings 8, 9 in conductive contact with both ends of a **diffuse layer resistor** 4 as a P-well formed on a N-type isolated insular region 10 are formed as round ends 8b, 9b, and the contact holes are formed not as square shape but round shape contact holes 4c, 4d. Thus, since no edge exists at the junctions between the resistor 4 and the wirings 8, 9, even if an overvoltage is applied to an input terminal 3, there is no electric field concentration, but there is a uniform electric field distribution. Thus, the breakdown voltage resistance of a wiring film is **enhanced**, and its current capacity is also increased.

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IC ICM H01L027-092  
ICS H01L027-04; H01L029-44; H01L029-784

=> file wpix  
FILE 'WPIX'  
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FILE LAST UPDATED: 10 APR 2003 <20030410/UP>  
MOST RECENT DERWENT UPDATE: 200324 <200324/DW>  
DERWENT WORLD PATENTS INDEX SUBSCRIBER FILE, COVERS 1963 TO DATE

=> d l205 1-5 max

L205 ANSWER 1 OF 5 WPIX (C) 2003 THOMSON DERWENT  
 AN 1994-152792 [19] WPIX  
 DNN N1994-120016 DNC C1994-070133  
 TI Mfg. **semiconductor device** with buried contact structure - involving cleaning after fluorine etching to avoid aluminium **wiring** defects.  
 DC L03 U11  
 IN KAJIYANA, K; YAMADA, Y  
 PA (NIDE) NEC CORP; (NIDE) NIPPON DENKI CO LTD  
 CYC 7  
 PI EP 596364 A2 19940511 (199419)\* EN 8p H01L021-74 <--  
     R: DE FR GB NL  
 JP 06140372 A 19940520 (199425) 6p H01L021-302 <--  
 EP 596364 A3 19940629 (199527) H01L021-74 <--  
 EP 596364 B1 19970312 (199715) EN 8p H01L021-74 <--  
     R: DE FR GB NL

DE 69308727 E 19970417 (199721) H01L021-74 <--  
 US 5804505 A 19980908 (199843) H01L021-44 <--  
 KR 134331 B1 19980420 (200012) H01L021-28 <--  
**ADT EP 596364 A2 EP 1993-117253 19931025; JP 06140372 A JP 1992-288031  
 19921027; EP 596364 A3 EP 1993-117253 19931025; EP 596364 B1 EP  
 1993-117253 19931025; DE 69308727 E DE 1993-608727 19931025, EP  
 1993-117253 19931025; US 5804505 A Cont of US 1993-139749 19931022,  
 US 1996-679489 19960712; KR 134331 B1 KR 1993-22272 19931026**  
**FDT DE 69308727 E Based on EP 596364**  
**PRAI JP 1992-288031 19921027**  
**REP No-SR.Pub; 1.Jnl.Ref; EP 309274; EP 324198; EP 571691; JP 59003927;  
 US 4668335; US 4926237**  
**IC ICM H01L021-28; H01L021-302; H01L021-44; H01L021-74  
 ICS H01L021-3205; H01L021-321; H01L021-768; H01L021-90; H01L023-485**  
**AB EP 596364 A UPAB: 19940627**  
 A **semiconductor device** prodn. process involves  
 (i) forming a hole in an **interlayer** insulating film on a  
 semiconductor substrate; (ii) forming a metal layer including a  
**titanium nitride** layer on the insulating film and  
 hole wall surfaces; (iii) depositing tungsten on the  
**titanium nitride** layer to fill the hole and form a  
 blanket tungsten layer; (iv) back-etching the blanket tungsten layer  
 using a fluorine-contg. etching gas until the **titanium**  
**nitride** layer, covering the insulating film top surface, is  
 exposed to leave a tungsten plug filling the hole, (v) cleaning the  
**titanium nitride** layer to remove fluorine, and  
 (vi) forming an aluminium layer on the cleaned **titanium**  
**nitride** layer.  
 ADVANTAGE - The process allows prodn. of a buried tungsten  
 contact structure without leaving residual titanium fluoride on the  
 TiN layer, thus maintaining adhesion between the Al **wiring**  
 layer and the TiN layer and enhancing  
 reliability of the Al  
**wiring** layer.  
 Dwg.2d/3  
**ABEQ EP 596364 B UPAB: 19970410**  
 A method of producing a **semiconductor device**  
 comprising the steps of forming a hole (31, 32) in an insulating  
 film (23) covering a semiconductor substrate (21), said insulating  
 film (23) thereby having a first surface defining said hole (31, 32)  
 and a second surface extending in parallel to said semiconductor  
 substrate (21), forming a metallic layer (24, 25, 65) covering said  
 first and second surfaces of said insulating film (23) and the base  
 (21, 22, 8-1, 8-2) of said hole (31, 32) said metallic layer (24,  
 25, 65) including a **titanium nitride** layer (25,  
 65) constituting the surface portion of said metallic layer (24, 25,  
 65) including a **titanium nitride** layer (25, 65)  
 constituting the surface portion of said metallic layer (24, 25,  
 65), depositing tungsten on said **titanium nitride**  
 layer (25, 65) so as to fill said hole (31, 32) and to form a  
 blanket tungsten layer (26), etching said blanket tungsten layer  
 (26) by an etching gas including fluorine until said metallic layer

(24, 25, 65) covering said second surface of said insulating film (23) is exposed while a tungsten plug (26-1, 26-2) filling said hole (31, 32) remains, and forming an aluminum layer (27-1, 27-2) covering the said exposed **titanium nitride** layer (25, 65) and contacting said plug, characterized by further comprising the step of cleaning said exposed **titanium nitride** layer (25, 65) to remove fluorine (40) and/or any titanium fluoride therefrom and to provide a cleaned **titanium nitride** layer (25, 65) prior to forming said aluminum layer (25, 65).

Dwg.3/3

FS CPI EPI  
 FA AB; GI  
 MC CPI: L04-C07; L04-C10; L04-C12B  
 EPI: U11-C05D3; U11-C05G2C

L205 ANSWER 2 OF 5 WPIX (C) 2003 THOMSON DERWENT

AN 1993-155648 [19] WPIX

CR 1993-138177 [17]; 1993-147231 [18]

DNN N1995-115906 DNC C1995-068525

TI Insulating layer esp. inter-level insulation or protective film formation - esp. for **semiconductor device** mfr., includes exposing the layer to an alkoxy-fluoro metallic vapour, pref. an alkoxy-fluoro silane.

DC L03 U11

IN HOMMA, T

PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO

CYC 3

PI JP 05090249 A 19930409 (199319)\* 5p H01L021-316 <--  
 US 5405805 A 19950411 (199520)B 19p H01L021-441 <--  
 KR 9606961 B1 19960525 (199918) H01L021-316 <--

ADT JP 05090249 A JP 1991-250781 19910930; US 5405805 A US 1992-943069  
 19920910; KR 9606961 B1 KR 1992-16642 19920909

FDT US 5405805 A JP 05074747, JP 05082512

PRAI JP 1991-250781 19910930; JP 1991-234238 19910913; JP 1991-242239  
 19910924

IC ICM H01L021-316; H01L021-441

AB US 5405805 A UPAB: 19950530 ABEQ treated as Basic  
 The multi-level **wiring** structure is obtd. by forming insulating films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub> or ZrO<sub>2</sub> or (organic) layers contg. these. At least part of the insulating film is exposed to an alkoxyfluorometal cpd. pref. an alkoxyfluoro- Si, -Ta, -Zr, -Ti, -Hf or -Al.

The layer is pref. SiO<sub>2</sub> or contains SiO<sub>2</sub>; and the vapour is an alkoxyfluorosilane.

ADVANTAGE - Water content of the insulating **layer** is reduced, enhancing device reliability and yield. (Issued in week 9520. First major country equivalent to JP5090249A).

Dwg.4G/12

AB JP 05090249 A UPAB: 19990511

The multi-level **wiring** structure is obtd. by forming insulating films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub> or ZrO<sub>2</sub> or

(organic) layers contg. these. At least part of the insulating film is exposed to an alkoxyfluorometal cpd. pref. an alkoxyfluoro- Si, - Ta, -Zr, -Ti, -Hf or -Al.

The layer is pref. SiO<sub>2</sub> or contains SiO<sub>2</sub>; and the vapour is an alkoxyfluorosilane.

**ADVANTAGE** - Water content of the insulating **layer** is reduced, **enhancing** device reliability and yield. (Issued in week 9520. First major country equivalent to JP5090249A).

Dwg.1/6

FS CPI EPI  
FA AB; GI  
MC CPI: L04-C13A  
EPI: U11-C05B7; U11-C05B9; U11-C05D2

L205 ANSWER 3 OF 5 WPIX (C) 2003 THOMSON DERWENT  
 AN 1993-147231 [18] WPIX  
 CR 1993-138177 [17]; 1993-155648 [19]  
 DNN N1993-112717 DNC C1993-065608  
 TI Insulating **layer** esp. inter-level insulation or protective film formation - esp. for **semiconductor** device mfr., includes exposing the layer to an alkoxy-fluoro metallic vapour, pref. an alkoxy-fluoro silane.  
 DC L03 U11  
 IN HOMMA, T  
 PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO  
 CYC 3  
 PI JP 05082512 A 19930402 (199318)\* 4p H01L021-316 <--  
 US 5405805 A 19950411 (199520)B 19p H01L021-441 <--  
 KR 9606961 B1 19960525 (199918) H01L021-316 <--  
 ADT JP 05082512 A JP 1991-242239 19910924; US 5405805 A US 1992-943069  
 19920910; KR 9606961 B1 KR 1992-16642 19920909  
 FDT US 5405805 A JP 05074747, JP 05082512  
 PRAI JP 1991-242239 19910924; JP 1991-234238 19910913; JP 1991-250781  
 19910930  
 IC ICM H01L021-316; H01L021-441  
 ICS H01L021-3105; H01L021-312  
 AB US 5405805 A UPAB: 19950530 ABEQ treated as Basic  
 The multi-level **wiring** structure is obtd. by forming insulating films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub> or ZrO<sub>2</sub> or (organic) layers contg. these. At least part of the insulating film is exposed to an alkoxyfluorometal cpd. pref. an alkoxyfluoro- Si, - Ta, -Zr, -Ti, -Hf or -Al.  
 The layer is pref. SiO<sub>2</sub> or contains SiO<sub>2</sub>; and the vapour is an alkoxyfluorosilane.  
**ADVANTAGE** - Water content of the insulating **layer** is reduced, **enhancing** device reliability and yield. (Issued in week 9520. First major country equivalent to JP5090249A).  
 Dwg.4G/12  
 AB JP 05082512 A UPAB: 19990511  
 The multi-level **wiring** structure is obtd. by forming insulating films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub> or ZrO<sub>2</sub> or (organic) layers contg. these. At least part of the insulating film

is exposed to an alkoxyfluorometal cpd. pref. an alkoxyfluoro- Si, - Ta, -Zr, -Ti, -Hf or -Al.

The layer is pref. SiO<sub>2</sub> or contains SiO<sub>2</sub>; and the vapour is an alkoxyfluorosilane.

ADVANTAGE - Water content of the insulating **layer** is reduced, **enhancing** device reliability and yield. (Issued in week 9520. First major country equivalent to JP5090249A).

FS CPI EPI

FA AB

MC CPI: L04-C12; L04-C13A

EPI: U11-C05A1; U11-C05B9; U11-C05D2

L205 ANSWER 4 OF 5 WPIX (C) 2003 THOMSON DERWENT

AN 1993-138177 [17] WPIX

CR 1993-147231 [18]; 1993-155648 [19]

DNN N1995-115906 DNC C1995-068525

TI Insulating **layer** esp. inter-level insulation or protective film formation - esp. for **semiconductor device** mfr., includes exposing the layer to an alkoxy-fluoro metallic vapour, pref. an alkoxy-fluoro silane.

DC L03 U11

IN HOMMA, T

PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO

CYC 3

PI JP 05074747 A 19930326 (199317)\* 4p H01L021-302 <--  
US 5405805 A 19950411 (199520)B 19p H01L021-441 <--  
KR 9606961 B1 19960525 (199918) H01L021-316 <--

ADT JP 05074747 A JP 1991-234238 19910913; US 5405805 A US 1992-943069  
19920910; KR 9606961 B1 KR 1992-16642 19920909

FDT US 5405805 A JP 05074747, JP 05082512

PRAI JP 1991-234238 19910913; JP 1991-242239 19910924; JP 1991-250781  
19910930

IC ICM H01L021-302; H01L021-316; H01L021-441

ICS H01L021-306; H01L023-522

AB US 5405805 A UPAB: 19950530 ABEQ treated as Basic  
The multi-level **wiring** structure is obtd. by forming  
insulating films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub> or ZrO<sub>2</sub> or  
(organic) layers contg. these. At least part of the insulating film  
is exposed to an alkoxyfluorometal cpd. pref. an alkoxyfluoro- Si, -  
Ta, -Zr, -Ti, -Hf or -Al.

The layer is pref. SiO<sub>2</sub> or contains SiO<sub>2</sub>; and the vapour is an alkoxyfluorosilane.

ADVANTAGE - Water content of the insulating **layer** is reduced, **enhancing** device reliability and yield. (Issued in week 9520. First major country equivalent to JP5090249A).

Dwg.4G/12

AB JP 05074747 A UPAB: 19990511

The multi-level **wiring** structure is obtd. by forming  
insulating films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub> or ZrO<sub>2</sub> or  
(organic) layers contg. these. At least part of the insulating film  
is exposed to an alkoxyfluorometal cpd. pref. an alkoxyfluoro- Si, -  
Ta, -Zr, -Ti, -Hf or -Al.

The layer is pref. SiO<sub>2</sub> or contains SiO<sub>2</sub>; and the vapour is an alkoxyfluorosilane.

**ADVANTAGE** - Water content of the insulating **layer** is reduced, **enhancing** device reliability and yield. (Issued in week 9520. First major country equivalent to JP5090249A).

Dwg.1/3

FS CPI EPI  
 FA AB; GI  
 MC CPI: L04-C07; L04-C10A; L04-C12A; L04-C12D; L04-C13A  
 EPI: U11-C05B9; U11-C05D1; U11-C05D2

L205 ANSWER 5 OF 5 WPIX (C) 2003 THOMSON DERWENT

AN 1988-148918 [22] WPIX

DNN N1988-113746

TI **Integrated circuit** with two or more aluminium metallisation planes - has specified metallic **inter-layer** by contact zone and silicide layers on metallisation planes.

DC U11

IN KUCHER, P; KUECHER, P

PA (SIEI) SIEMENS AG

CYC 11

PI EP 269095 A 19880601 (198822)\* DE 8p <--  
 R: AT BE CH DE FR GB IT LI NL  
 JP 63142835 A 19880615 (198830) <--  
 US 4924295 A 19900508 (199023) <--  
 EP 269095 B1 19940216 (199407) DE 13p H01L023-532 <--  
 R: AT BE CH DE FR GB IT LI NL  
 DE 3789090 G 19940324 (199413) H01L023-532 <--

ADT EP 269095 A EP 1987-117415 19871125; JP 63142835 A JP 1987-295951  
 19871124; US 4924295 A US 1987-107344 19871013; EP 269095 B1 EP  
 1987-117415 19871125; DE 3789090 G DE 1987-3789090 19871125, EP  
 1987-117415 19871125

FDT DE 3789090 G Based on EP 269095

PRAI DE 1986-3640656 19861128

REP 3.Jnl.Ref; A3...9032; No-SR.Pub; 1.Jnl.Ref; EP 127281; EP 211318; US 4566026

IC H01L021-60; H01L023-48

ICM H01L023-532

ICS H01L021-60; H01L021-90; H01L023-48

AB EP 269095 A UPAB: 19930923

A first metallic intermediate layer (5) of tungsten silicide, titanium/tungsten, titanium/tungsten **nitride** or **titanium nitride** is beside the silicon zone (14) to be contacted. On each of a set of insulated, separated metallisation planes (8,18,28) are arranged further covering layers of metal silicide intermediate layers. As seeding layer for the metallisation planes are intermediate layers (7,17,27) with improved electron-migration-withstand capability over aluminium.

Pref. the covering layers consist of molybdenum silicide and the seeding layers are of a double layer of titanium/titanium **nitride**. The **titanium nitride** is around

five times as thick as the titanium.

**USE/ADVANTAGE** - VLSI circuits. Enables line separations in sub-micron region, with high planarity of metallisation and consequent space-saving. High stability of **wiring** with resistance to electron migration and no thermal stress or corrosion.  
3/4

ABEQ US 4924295 A UPAB: 19930923

The circuit comprises at least two metallisation levels composed of aluminium or of an aluminum contact. Tungsten is used as a via hole filler and metal silicides are used as intermediate layers. The metallisation pattern contains a nucleation layer pref. composed of titanium/titanium m nitride as an under-layer for every metallisation level.

The electron migration resistance of the aluminum **layers** is enhanced and a **layer** preferably composed of molybdenum silicide is used as a cover layer for every metallisation level, thus improving the low-impedance of the metallisation.

**USE/ADVANTAGE** - Sandwich-like metallisation structure improves planarity and thermal stability of circuit. Since number of metallisation levels is arbitrary, structure can be used for **VLSI** circuits.

ABEQ EP 269095 B UPAB: 19940329

#### **Integrated semiconductor circuit**

having a substrate (1) which comprises silicon and in which and on which the elements forming the circuit are created, having a first insulating layer (2) which is disposed on the substrate and is provided with contact vias (3), and having at least two metallisation levels (8, 18, 28) which comprise aluminium or an aluminium compound and are separated by a further insulating layer (10, 20) provided with contact vias (13) and which are connected to one another and to the regions (4), to be contacted, in and on the silicon substrate (1) using contact via fillers (6, 16, 26) comprising tungsten, a metal silicide **interlayer** (9, 19) being disposed as covering layer on each metallisation level (8, 18, 28), characterised by: (a) a first metal **interlayer** (5) composed of tungsten silicide (WSix) or titanium-tungsten, titanium-tungsten nitride or titanium nitride which is disposed between the lowermost contact via fillers (6) and the substrate regions (4) to be contacted, and (b) an **interlayer** (7, 17, 27) which serves as nucleation layer for the aluminium metallisation and is disposed in each case beneath a metallisation level, the **interlayer** (7, 17, 27) comprising a Ti-TiN double layer having a defined microstructure, with the result that, to increase the electromigration resistance, the aluminium metallisation level (8, 18, 28) situated on top of the **interlayer** has a strong (111) preferred orientation with homogeneous crystallite-size distribution.

Dwg.1/4

FS

EPI

FA

AB; GI

MC

EPI: U11-C05D2; U11-D03B2

=> d 1206 1-7 max

L206 ANSWER 1 OF 7 WPIX (C) 2003 THOMSON DERWENT  
 AN 2000-259734 [23] WPIX  
 DNN N2000-193277 DNC C2000-079715  
 TI **Multilayered wiring structure for semiconductor device** manufacture, includes alpha phase **tantalum** and aluminum alloy conductive layers sequentially formed on silicon dioxide film.  
 DC L03 U11  
 IN KONO, T  
 PA (FUIT) FUJITSU LTD  
 CYC 2  
 PI JP 11340228 A 19991210 (200023)\* 6p H01L021-3205 <--  
 US 6232664 B1 20010515 (200129) H01L023-48  
 ADT JP 11340228 A JP 1998-148010 19980528; US 6232664 B1 US 1999-227263  
 19990108  
 PRAI JP 1998-148010 19980528  
 IC ICM H01L021-3205; H01L023-48  
 AB JP 11340228 A UPAB: 20000516  
 NOVELTY - A silicon dioxide film (2) is formed on a silicon substrate (1) on which **semiconductor device** is formed. **Semiconductor device** comprises **wiring** which includes pair of conductive layers (4,5). The conductive layers consist of **tantalum** of alpha phase and aluminum alloy, respectively. DETAILED DESCRIPTION - A **semiconductor device** formed on a silicon substrate is connected electrically to the **wiring** through the conducting material embedded in the contact hole provided in the silicon dioxide film.  
 USE - For **semiconductor device** manufacture.  
 ADVANTAGE - Alpha phase **tantalum** film enhances orientation of aluminum alloy film, thus electromigration resistance of **wiring** is enhanced.  
 DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **wiring** layer explaining the manufacturing process of **wiring** structure. (1) Silicon substrate; (2) Silicon dioxide film; (4,5) Conductive layers.  
 Dwg.2/5  
 FS CPI EPI  
 FA AB; GI  
 MC CPI: L04-C10A  
 EPI: U11-C05  
 L206 ANSWER 2 OF 7 WPIX (C) 2003 THOMSON DERWENT  
 AN 2000-045951 [04] WPIX  
 DNN N2000-035526  
 TI **Multilayered structure of printed wiring board** - has center substrate layer, double-sides layers and laminated **multilayer**, whose thickness are set to

specific value.

DC V04  
 PA (ITOK-I) ITO K; (TOHO-N) TOHOKU RIKO KK  
 CYC 1  
 PI JP 11307894 A 19991105 (200004)\* 8p H05K001-09 <--  
 ADT JP 11307894 A JP 1998-116619 19980427  
 PRAI JP 1998-116619 19980427  
 IC ICM H05K001-09  
 ICS H05K001-02  
 AB JP 11307894 A UPAB: 20000124

NOVELTY - Signal layer (12) with power supply patterns, earthing layer (13), power supply layer (14) and signal layer (15) with earthing patterns are laminated sequentially. The thickness (t0) of center substrate layer (16), thickness (t1) of double-sided layers (17,18) and thickness (ta) of **laminated multilayer** are set to specific value.

USE - In **printed wiring board** of electronic machine such as office automation apparatus, personal computer, household electric appliances, etc.

ADVANTAGE - Noise reduction effect can be redoubled without providing extra component and thereby reduces the cost. Also the **laminated structure enhances** noise suppression by 30% or more. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the **multilayered** structure of PCB. (12,15) Signal layers; (13) Earthing layer; (14) Power supply layer; (16) Center substrate.

Dwg.2/9

FS EPI  
 FA AB; GI  
 MC EPI: V04-Q05; V04-R02P

L206 ANSWER 3 OF 7 WPIX (C) 2003 THOMSON DERWENT  
 AN 1999-620865 [53] WPIX  
 DNN N1999-457921 DNC C1999-181338  
 TI Fabricating **semiconductor integrated**  
 circuit chip structures for microprocessors and  
 digital signal processors.  
 DC L03 U11  
 IN MOSLEHI, M M; MOSLEHI, M  
 PA (CVCC-N) CVC INC; (CVCC-N) CVC PROD INC  
 CYC 21  
 PI WO 9954934 A1 19991028 (199953)\* EN 78p H01L023-48 <--  
 RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE  
 W: JP KR  
 US 6016000 A 20000118 (200011) H01L029-00  
 EP 1000440 A1 20000517 (200028) EN H01L023-48  
 R: DE FR GB IT NL  
 US 6124198 A 20000926 (200051) H01L021-768  
 KR 2001020476 A 20010315 (200159) H01L023-48  
 JP 2002506577 W 20020226 (200219) 54p H01L021-768  
 ADT WO 9954934 A1 WO 1999-US8475 19990422; US 6016000 A US 1998-64431  
 19980422; EP 1000440 A1 EP 1999-917606 19990422, WO 1999-US8475

19990422; US 6124198 A Div ex US 1998-64431 19980422, US 1998-187297  
19981105; KR 2001020476 A KR 1999-712124 19991222; JP 2002506577 W  
JP 1999-553180 19990422, WO 1999-US8475 19990422  
FDT EP 1000440 A1 Based on WO 9954934; US 6124198 A Div ex US 6016000;  
JP 2002506577 W Based on WO 9954934  
PRAI US 1998-187297 19981105; US 1998-64431 19980422  
IC ICM H01L021-768; H01L023-48; H01L029-00  
ICS H01L021-316; H01L021-318; H01L021-4763; H01L023-52; H01L029-40  
AB WO 9954934 A UPAB: 19991215

NOVELTY - An ultra-high-speed multilevel chip interconnect structure using a free-space dielectric medium is provided for a **semiconductor integrated circuit (IC)** chip.

DETAILED DESCRIPTION - A multilevel interconnect structure for a **semiconductor IC chip** for a **semiconductor substrate** comprises:

(a) electrically conductive metallization levels with interconnect segments;

(b) plugs for connecting various metallization levels and the **semiconductor devices**;

(c) a free-space medium occupying at least a portion of the electrically insulating regions within the multilevel interconnect structure; and

(d) an electrically insulating top passivation overlayer for hermetic sealing and for protection of the **IC chip**, which also serves as a heat transfer medium for facilitating heat removal from the interconnect structure and provides mechanical support for interconnect structure through contact with the top metallization level of the multilevel interconnect structure.

An INDEPENDENT CLAIM is also included for a method for the fabrication of a multilevel interconnect structure.

USE - The method is used for the fabrication of **semiconductor IC chips** to be use in microprocessors and digital signal processors (DSP).

ADVANTAGE - The invention offers improved interconnect structures and methods which will reduce the parasitic effects and enhance the **semiconductor integrated circuit** speed and operational reliability. Simplification at the interconnect process is enabled and chip manufacturing cost is reduced. The invention provides the use of a free-space interlevel/intermetal dielectric (ILD/IMD) medium. It is compatible with **damascene** (single /dual) interconnect fabrication process with a reduced number of process steps per interconnect by four steps. Its compatibility is applicable to various types of interconnect metallization materials such as copper, gold, silver, aluminum, and other superconducting materials. It provides excellent thermal management and efficient heat dissipation removal capabilities. The interconnect structure provides reduce RC propagation delay and reduced capacitive crosstalk. Interconnect metallization electromigration lifetime is improved. It neglects the use of low-k dielectric materials, relatively complex and expensive process integration methods. The invention provides hermetic sealing

of the multilevel interconnect structure and **semiconductor IC devices**. It also provides excellent mechanical strength and integrity of the multilevel interconnect structure and overall **semiconductor chip** (claimed).

DESCRIPTION OF DRAWING(S) - The drawing shows a multilevel interconnect structure following formation of an etchant-transmission window pattern on the top layer and after formation of a free-space dielectric medium.

Dwg.13/15

TECH WO 9954934 A1 UPTX: 19991215

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Materials: A portion of an electrically conductive interconnect segments and plugs are made of high electrical conductivity materials or superconducting materials. The top passivation overlayer and bottom insulating buffer layer are formed using at least one etch-resistant electrically insulating material. The disposable inter-level and inter-metal material layers is silicon oxide. The insulating bottom buffer layer is made of silicon nitride, aluminum nitride, diamond-like coating, silicon carbide or boron nitride.

Preferred Free-space Medium: The hermetic sealed free-space medium is made of a gaseous material in a vacuum at atmospheric pressure or less than 5 atmospheres. The gaseous material comprises a high thermal conductivity inert gas preferably helium, argon, nitrogen or hydrogen. The gaseous material suppresses electrical leakage currents and gas breakdown within the medium due to electrically conductive interconnect segments and plugs.

Preferred Structures: Electrically insulating bottom buffer layer separates the multilevel interconnect structure from underlying transistors and isolation regions fabricated within the **semiconductor IC chip** substrate. It

provides mechanical support for the multilevel interconnect structure. It provides a blocking material with effective diffusion barrier properties against contamination of the substrate by the metallization materials and ionic contaminants. It enables the formation of free-space medium without damage to underlying transitory and isolation regions.

The insulating top passivation overlayer comprises a material layer with several open bonding pad

windows which is used for the formation of free-space medium and hermetic sealing of the interconnect structure while the insulating bottom buffer provides openings for electrical connections between plugs and underlying transition within the semiconductor substrate. The electrically conductive levels and plugs are embedded within a sealed cavity formed between top passivation overlayer and bottom buffer layer in conjunction with a free-space dielectric medium. The plugs which provide electrical connection between the first metallization level and underlying **semiconductor devices** are encapsulated in a conductive diffusion barrier layer (such as TiNx, TaNx, WN<sub>x</sub>, Ta, or ternary conductive barrier material), while the second to the top level do not utilize any conductive diffusion barrier layers.

The interconnect segments comprise an encapsulation coating layer of

an electrically conductive material (such as TiNx, TaNx, or silver) that suppresses electrical leakage within the interconnect structure. At least a portion of contact interfaces among conductive metallization levels and plugs comprises of identical metallization materials without any interfacial contact barrier layer. A dummy plug connected to the bottom surface of the top passivation overlayer provides structural and mechanical support for the multilevel interconnect structure.

**Preferred Encapsulation Coating Layer:** The insulating material is silicon dioxide, silicon nitride, aluminum nitride, aluminum oxide, or diamond-like carbon. **Preferred Method:** The multilevel interconnect structure is formed using 2N+1 micro lithography masking steps for N metallization levels. The metallization levels and electrically conductive plugs are formed within disposable material layers using **damascene** process flow. A high electrical conductivity material is deposited using chemical-vapor deposition, physical-vapor deposition and/or electroplating.

ABEX WO 9954934 A1 UPTX: 19991215

**SPECIFIC MATERIALS** - At least a portion of an electrically conductive interconnect segments and plugs are made of copper, aluminum or silver. The semiconductor substrate is made of silicon, silicon-on-insulator or gallium arsenide. The insulating top passivation overlayer is made of silicon nitride, silicon oxynitride, aluminum nitride, diamond-like coating, boron nitride or silicon carbide.

FS CPI EPI

FA AB; GI

MC CPI: L04-C10; L04-C12; L04-C13; L04-F

EPI: U11-C05B9A; U11-C05D1; U11-C05D3; U11-D03B2

DRN 1247-U; 1893-U

L206 ANSWER 4 OF 7 WPIX (C) 2003 THOMSON DERWENT

AN 1999-459900 [39] WPIX

DNN N1999-344069 DNC C1999-135251

TI **Semiconductor device copper wiring**

production especially for highly integrated power semiconductor device.

DC L03 U11

IN HWANG, Y; KIM, D; KIM, J; LEE, S; PARK, C; RHA, S; HWANG, Y S; KIM, D W; KIM, J G; LEE, S Y; PARK, J W; RAH, S G

PA (GLDS) LG SEMICON CO LTD; (HYUN-N) HYUNDAI MICROELECTRONICS CO LTD; (GLDS) LG SEMICONDUCTOR CO LTD

CYC 5

PI DE 19843173	A1 19990819 (199939)*	6p	H01L021-768	<--
JP 11274159	A 19991008 (199954)	4p	H01L021-3205	<--
US 6057228	A 20000502 (200029)		H01L021-00	
KR 99069376	A 19990906 (200046)		H01L021-28	<--
TW 383478	A 20000301 (200051)		H01L023-50	
KR 259357	B1 20000615 (200131)		H01L021-28	

ADT DE 19843173 A1 DE 1998-19843173 19980921; JP 11274159 A JP 1999-29761 19990208; US 6057228 A US 1998-140834 19980826; KR 99069376 A KR 1998-3580 19980207; TW 383478 A TW 1998-114421

PRAI 19980831; KR 259357 B1 KR 1998-3580 19980207  
 PRAI KR 1998-3580 19980207  
 IC ICM H01L021-00; H01L021-28; H01L021-3205; H01L021-768; H01L023-50  
 ICS H01L021-28  
 AB DE 19843173 A UPAB: 19990928  
**NOVELTY - A semiconductor device wiring**  
 is formed by melting a thin copper film (30), applied on an insulating layer (20) with a trench (21), in a halogen-containing atmosphere.  
**DETAILED DESCRIPTION - Preferred Features:** The halogen is selected from fluorine, chlorine, bromine and **iodine**. Fluorine or chlorine is implanted in the gaseous state. Bromine or **iodine** is supplied in liquid form and is converted to the gaseous state using a bubbler or using liquid MFC and an evaporator.  
**USE -** Especially to produce a copper **wiring** for a highly integrated power **semiconductor device**.  
**ADVANTAGE -** The use of a halogen-containing atmosphere allows formation of the copper **wiring** using a lower annealing temperature and a shorter annealing time compared with prior art processes which use an oxygen/hydrogen atmosphere (i.e. less than 30 minutes at below 450 deg. C compared with more than 1 hour at greater than or equal to 500 deg. C), thus **reducing copper diffusion** into the device and increasing productivity.  
**DESCRIPTION OF DRAWING(S) -** The drawing shows a vertical cross-sectional view of formation of a copper **wiring**.  
 Semiconductor substrate 10  
 Insulating layer 20  
 Trench 21  
 Thin copper film 30  
 Dwg. 4/6  
 FS CPI EPI  
 FA AB; GI  
 MC CPI: L04-C10A; L04-C10D  
 EPI: U11-C05D; U11-C05D3  
 L206 ANSWER 5 OF 7 WPIX (C) 2003 THOMSON DERWENT  
 AN 1998-551428 [47] WPIX  
 DNN N1998-430251 DNC C1998-165284  
 TI Surface treating agent for copper and copper alloy - consists of an aqueous solution containing a 2-(arylmethyl)benzimidazole compound and **iodine** ions.  
 DC E13 L03 M14 V04  
 PA (SHIJ) SHIKOKU KASEI KOGYO KK  
 CYC 1  
 PI JP 10245684 A 19980914 (199847)\* 6p C23C022-52 <--  
 ADT JP 10245684 A JP 1997-69300 19970305  
 PRAI JP 1997-69300 19970305  
 IC ICM C23C022-52  
 ICS H05K003-34  
 AB JP 10245684 A UPAB: 19981210  
 A surface treating agent consists of an aqueous solution containing

a 2-(aryl methyl)benzimidazole compound of formula (I), and 10-150 ppm-**iodine** ions as its essential constituents. In formula (I), R1, R2 = hydrogen atoms, or halogen atoms; and R1 and R2 are not simultaneously hydrogen atoms.

**USE** - The surface treating agent finds its application in preflux for a copper circuit on a hard **printed wiring board**, or a flexible **printed wiring board**.

**ADVANTAGE** - The surface treating agent has superior heat resistance, and less decrease in film-formation rate with respect to copper. The use of the aqueous solution described above enhances film properties, including wetting time, and cream solder spread.

Dwg.0/0

FS CPI EPI

FA AB; GI; DCN

MC CPI: E06-D05; E31-B03C; L03-H04E6; M14-D

EPI: V04-R04A

CMC UPB 19981223

M3 \*01\* D012 D711 G011 G012 G013 G014 G015 G016 G100 H6 H601 H602  
H603 H604 H608 H641 H642 M1 M123 M132 M280 M311 M321 M342  
M412 M511 M520 M531 M540 M781 M903 M904 Q454 Q465  
DCN: 9847-EPS01-K; 9847-EPS01-U

L206 ANSWER 6 OF 7 WPIX (C) 2003 THOMSON DERWENT

AN 1993-170672 [21] WPIX

DNN N1993-130937 DNC C1993-076066

TI Film-forming **titanium nitride** film for prodn. of **semiconductor device** - comprises forming titanium film and heating in nitriding atmos. to form granular fine crystal structure.

AW CARBON.

DC L03 M13 U11

PA (MITQ) MITSUBISHI ELECTRIC CORP

CYC 1

PI JP 05102328 A 19930423 (199321)\* 6p H01L021-09 <--

ADT JP 05102328 A JP 1991-257609 19911004

PRAI JP 1991-257609 19911004

IC ICM H01L021-09

ICS C01B021-06; H01L021-318; H01L021-3205

AB JP 05102328 A UPAB: 19931114

Formation comprises (a) film-forming a Ti film on a substrate; and (b) applying heat treatment to the Ti film in nitriding atmos. to form a **Ti nitride** film having granular fine crystal structure.

Prodn. of a **semiconductor device** comprises (a) film-forming a Ti layer; (b) applying heat treatment to the Ti layer in nitriding atmos. to form a **Ti nitride** layer having granular fine crystal structure; and (c) forming a **wiring** layer. In the **semiconductor device**, the **wiring** layer is formed through a barrier layer on the semiconductor substrate. The barrier layer pref. has the

**Ti nitride layer.**

USE/ADVANTAGE - Use of the **titanium nitride** layer for the barrier layer prevents substrate atoms from diffusing into the **wiring layer**, allowing flatness processing after forming the **wiring layer**. The result enhances yield and reliability in producing the **multilayered wiring structure high-integrated semiconductor device**.

Dwg.3/6

FS CPI EPI

FA AB; GI

MC CPI: L04-C12B; M13-D03B

EPI: U11-C05B4; U11-C05B6; U11-C05D3; U11-D03B2

L206 ANSWER 7 OF 7 WPIX (C) 2003 THOMSON DERWENT

AN 1986-145437 [23] WPIX

DNN N1986-107679 DNC C1986-062175

TI Formation of semiconductor **IC** - includes forming contact holes in insulating film over device region and implanting region through holes.AW **INTEGRATE CIRCUIT.**

DC L03 U11 U13

IN IKEDA, S; MEGURO, S; MOTOYOSHI, M; NAGAI, K; NAGASAWA, K

PA (HITA) HITACHI LTD; (YKED-I) YKEDA S

CYC 8

PI EP 183204 A 19860604 (198623)\* EN 23p &lt;--

R: DE FR GB IT

JP 61125166 A 19860612 (198630) &lt;--

JP 61182254 A 19860814 (198639) &lt;--

CN 85109742 A 19860709 (198712) &lt;--

US 4734383 A 19880329 (198816) &lt;--

US 5055420 A 19911008 (199143) &lt;--

KR 9406668 B1 19940725 (199619) H01L021-265 &lt;--

ADT EP 183204 A EP 1985-114857 19851121; JP 61125166 A JP 1984-246028  
19841122; JP 61182254 A JP 1985-21673 19850208; US 4734383 A US  
1985-800954 19851122; US 5055420 A US 1989-351323 19890509; KR  
9406668 B1 KR 1985-8576 19851116

PRAI JP 1984-246028 19841122; JP 1985-21673 19850208

REP 1.Jnl.Ref; A3...8806; FR 2372511; GB 2034974; No-SR.Pub; US 4046607;  
US 4435896

IC H01L021-82; H01L027-08; H01L029-78

ICM H01L021-265

ICS H01L021-82; H01L027-08; H01L029-78

AB EP 183204 A UPAB: 19930922

**Semiconductor IC device** is formed by:

forming an n-channel MOSFET having an n-region and a p-channel MOSFET having a p-region; covering with an insulation film; forming on each of the n and p regions; and ion implanting n-impurity into at least the n-region through the contact holes.

Pref. a second insulating film is added after formation of the contact holes and the impurity is implanted through the film.

n-impurity is implanted into teh n and p regions, the implanted

concn. in the p-region being below the p-impurity concn. A photoresist mask is used for the implantation. The n-impurity is P. The second insulating film is Si oxide formed by oxidising exposed substrate; this film prevents outward diffusion of the n-impurity during the post-implant anneal. Other contact holes are formed over a polySi wiring layer formed on the substrate.

**ADVANTAGE** - Method avoids destruction of junctions and reduces resistance between a semiconductor region and a conductive layer to enhance device speed.

1/6

ABEQ US 4734383 A UPAB: 19930922

Integrated circuit is formed with an n-channel MOSFET with n-type regions and a p-channel MOSFET with p-type regions on a semiconductor substrate. The MOSFETs are covered with an insulating film and at least two contact holes are formed in the insulating film, respectively in each MOSFET area. A second insulating film is applied to cover the surface of the substrate exposed to the outside through the contact holes. An impurity is implanted into the n-type region and annealing carried out, so that a further deeper n-type region is formed. The second insulating film is removed and a conductive film formed in the contact holes.

**ADVANTAGE** - The circuit can be made without any junction being easily destroyed, without an increase in the number of mfg. steps.

ABEQ US 5055420 A UPAB: 19930922

The process comprises (a) forming a 1st insulating film covering N-channel and P-channel MOSFETs provided on a main surface of a semiconductor substrate, the MOSFETs having n-type and p-type regions respectively, (b) simultaneously forming at least two contact holes in the 1st insulating film to at least each n- and p-type region, (c) forming a mask covering at least one contact hole on the p-type region, (d) introducing an n-type impurity into at least the n-type region through at least one of the contact holes, and annealing so as to provide a further n-type region that extends deeper, and (e) forming a conductive film in the contact holes.

**ADVANTAGE**- Junctions are prevented from being easily destroyed, without any large increase in the number of steps. Resistance at the connection between a semiconductor region and a conductive layer is reduced, thus increasing device operation speed. @@

FS CPI EPI

FA AB

MC CPI: L04-E

EPI: U11-C05C4; U13-D02A

DRN 1694-U

=> d 1207 1-4 max

DNN N2000-401593 DNC C2000-161484  
 TI Interconnection structure e.g., corrosion resistant integrated fuse includes a corrosion resistant metal barrier layer which separates a relatively low resistivity metal from a conductive **wiring**.  
 DC L03 U11  
 IN STAMPER, A K  
 PA (IBMC) INT BUSINESS MACHINES CORP  
 CYC 3  
 PI US 6111301 A 20000829 (200049)\* 6p H01L029-00  
     KR 99082726 A 19991125 (200055) H01L021-768 <--  
     TW 406391 A 20000921 (200127) H01L023-522  
     KR 329899 B 20020322 (200265) H01L021-768  
 ADT US 6111301 A US 1998-66121 19980424; KR 99082726 A KR 1999-8218  
     19990312; TW 406391 A TW 1999-101472 19990201; KR 329899 B KR  
     1999-8218 19990312  
 FDT KR 329899 B Previous Publ. KR 99082726  
 PRAI US 1998-66121 19980424  
 IC ICM H01L021-768; H01L023-522; H01L029-00  
     ICS H01L023-48; H01L023-52; H01L029-40  
 AB US 6111301 A UPAB: 20001006  
 NOVELTY - Interconnection structure includes a fuse structure consisting of a relatively low resistivity metal which is electrically connected to a conductive **wiring** located on a different level. A barrier layer of a corrosion resistant metal is located between the low resistivity metal and the **wiring** to separate the **wiring** from the low resistivity metal.

DETAILED DESCRIPTION - An interconnection structure for a **semiconductor circuit** includes a fuse structure and a conductive **wiring** located on a different level to the fuse structure. The fuse structure comprises a relatively low resistivity metal (2, 6) and is electrically connected to the conductive **wiring**. A conformal barrier layer (3) of a **chemical vapor deposited** corrosion resistant metal conductively contacts the low resistivity metal. The barrier layer is located intermediate the low resistivity metal and the **wiring** and along the sides of the low resistivity metal thereby separating the **wiring** from the low resistivity metal.

USE - Corrosion resistant integrated fuse for a **planar** copper back end of line (BEOL).

ADVANTAGE - The fuse structure consists of a relatively low resistivity metal such as copper that exhibits integrated corrosion stop. The fuse structure can be electrically interconnected directly to a **wiring** located on a different level without using an intermediate via to act as a corrosion barrier.

DESCRIPTION OF DRAWING(S) - The diagram illustrates an embodiment of the upper wire fuse in which the via is fabricated using single **damascene**.

Metal layers 2, 6

Copper corrosion barrier 3

Via 4

Dwg.3/5

TECH US 6111301 A UPTX: 20001006

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Structure: The low resistivity metal is located on the barrier layer. The fuse structure further comprises an adhesion promoting **layer** or a **diffusion barrier** between the low resistivity metal and the corrosion resistant metal. The interconnection structure further comprises a via between the different levels. The fuse structure is located in a trench in the interconnection structure and the conformal barrier layer is located adjacent the sidewalls and the bottom of the trench.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The adhesion promoting layer includes **tantalum nitride**. The low resistivity metal is copper and the corrosion resistant metal is tungsten preferably **chemical vapor deposited** tungsten.

FS CPI EPI

FA AB; GI

MC CPI: L04-C10; L04-E

EPI: U11-C05D3; U11-D03B2A

L207 ANSWER 2 OF 4 WPIX (C) 2003 THOMSON DERWENT

AN 2000-125717 [11] WPIX

DNN N2000-094728 DNC C2000-038178

TI Conducting metal line and interconnect formation for use in trenches and vias in the fabrication of **integrated circuit** devices that forms a Chemical Mechanical Polish (**CMP**) **planarized** structure without dishing.

DC L03 P61 U11

IN ROY, S R

PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

CYC 2

PI	US 6004188	A 19991221 (200011)*	8p	B24B001-00	<--
	SG 72907	A1 20000523 (200033)		B24B001-00	

ADT US 6004188 A US 1998-151153 19980910; SG 72907 A1 SG 1998-5572  
19981211

PRAI US 1998-151153 19980910

IC ICM B24B001-00

AB US 6004188 A UPAB: 20000301

NOVELTY - Method of forming conducting metal lines and interconnects in trenches and vias in the fabrication of **integrated circuit** devices that forms chemical mechanical polish (**CMP**) **planarized** structure without dishing employs the use of a special **CMP** dual **damascene** technique with a unique double **CMP** barrier layer (11).

DETAILED DESCRIPTION - Method of forming conducting metal lines and interconnects (studs) in trenches and vias in the fabrication of **integrated circuit** devices that forms **CMP** **planarized** structure without dishing, comprises providing a substrate upon which an insulator layer is deposited. A layer of first material is deposited upon the insulator layer. The first

material and insulator layer are patterned and etched to form via holes for interconnects and to form trenches for conducting lines. A conformal layer of second material is blanket deposited above the patterned layer of the first material and insulator layer. The second material is provided with a covering or lining of the trench and via structures. A blanket conducting metal is deposited over the entire substrate filling the open trench and via structures. The conducting metal layer is chemical-mechanical **polished** in a two-step process which includes **polishing** back the top metal layer with the second material layer which is harder than the conducting layer, and further **polishing** back the top metal layer with the first material layer which is preferably of soft material and close to the conducting material in **polishing** rate, thus forming **planarized** conducting metal line and interconnect structures, without dishing. All residual first material is removed from the two step process, and the second layer material is left as a liner and **diffusion barrier** in the trench/via structures.

**Preferred Layers:** The insulating oxide layer (10) is silicon oxide deposited by the method of polyethylene (PE) deposited tetraethyl orthosilicate (TEOS) oxide in the thickness of 4000-12000 Angstrom . The layer of first material is **titanium nitride** (TiN) deposited by plasma vapor deposition ( PVD) in a thickness of 300-1000 Angstrom . The layer (12) of second material is **tantalum/tantalum nitride** (Ta/TaN) deposited by PVD in a thickness of 200-500 Angstrom . The layer (14) of top conducting metal is preferably copper deposited by **chemical vapor deposition** (CVD) in a thickness of 10000-30000 Angstrom . Thin films of TiN, Ta, and TaN may also be deposited by CVD. TiN layer **polishing** properties have a faster removal rate than **Ta** or **TaN**. **Ta** or **TaN** has a slower **polishing** rate than copper. **TiN** forms a buffer layer for **Ta** or **TaN**. A combination of **Ta/TaN** forms a dual layer with **TiN** and acts as a **polishing barrier** to yield **planar** copper structures. The method uses the dual layers of **TiN**, **Ta/TaN** in a **damascene** process to **planarize** Cu lines and interconnects using **CMP**, with built-in **polishing stop** at the insulating material surface. The dual layer combined action **planarizes** the surface. The method using the dual **damascene** technique preferably forms a conductive contact to a semiconductor diffusion and interconnection **wiring** pattern in the fabrication of a metal oxide semiconductor field-effect transistor (MOSFET) that forms **CMP planarized** structures. Dual **damascene** process with dual **CMP** barrier layer is used, and contact is made to a conducting line in a multilevel metal connection structure on a semiconductor substrate (1).

**USE -** The invention is used for forming conducting metal lines and interconnects in trenches and vias in the fabrication of integrated circuit devices that forms **CMP**

**planarized structure.**

**ADVANTAGE -** The invented method provides uniformity across the substrate and better electrical performance due to the increased copper line cross-section. It avoids thinning of the conducting lines which increase line or **wire** resistance, and eliminates dishing of the copper lines and interconnects.

**DESCRIPTION OF DRAWING(S) -** The figure shows a substrate, semiconductor or multilevel metal with partially complete cross-section of a conducting line and interconnect.

**Substrate 1**

- Insulating material 10
- CMP barrier layer 11
- Ta or TaN layer 12
- Conducting metal layer 14

Dwg.2/6

FS CPI EPI GMPI

FA AB; GI

MC CPI: L04-C10A; L04-C13B; L04-C26

EPI: U11-C05D3; U11-C05G2C; U11-C06A1A

L207 ANSWER 3 OF 4 WPIX (C) 2003 THOMSON DERWENT

AN 1999-256780 [22] WPIX

DNN N1999-191342 DNC C1999-075349

TI Manufacturing **semiconductor device** with copper **wiring** film.

DC L03 U11

IN ONISHI, H

PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO

CYC 29

PI EP 913863 A2 19990506 (199922)\* EN 11p H01L023-485 <--  
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK

NL PT RO SE SI

JP 11135506 A 19990521 (199931) 6p H01L021-3205 <--

CN 1216398 A 19990512 (199937) H01L021-3205 <--

KR 99037442 A 19990525 (200032) H01L021-28 <--

TW 423076 A 20010221 (200138) H01L021-3205

ADT EP 913863 A2 EP 1998-119950 19981021; JP 11135506 A JP 1997-316089  
19971031; CN 1216398 A CN 1998-120479 19981026; KR 99037442 A KR  
1998-45358 19981028; TW 423076 A TW 1998-116767 19981008

PRAI JP 1997-316089 19971031

IC ICM H01L021-28; H01L021-3205; H01L023-485

ICS H01L021-60; H01L021-768

AB EP 913863 A UPAB: 19990609

**NOVELTY -** A copper **wiring** film (3) is formed in an **interlayer** insulating film (4-3) by a **damascene** method. A protective insulating film (6) is formed on the copper **wire** and **interlayer** insulator, then an opening made in the film into which an aluminum film (7) is deposited. A chemical mechanical polishing (CMP) process is performed to leave only aluminum in the opening.

**USE -** In the manufacture of a **semiconductor** device.

**ADVANTAGE** - The aluminum surface at a bond pad provides a better bonding performance during assembly.

**DESCRIPTION OF DRAWING(S)** - The drawing shows a cross section of the bond pad of a **semiconductor device**.

Silicon substrate 1

Titanium nitride 2-1, 2-2, 2-3

Copper 3

Silicon dioxide 4-1,4-2,4-3

Silicon nitride 5-2

Silicon nitride 6

Aluminum 7

Dwg.3/5

TECH EP 913863 A2 UPTX: 19990609

**TECHNOLOGY FOCUS - METALLURGY** - The aluminum containing film is selected from aluminum, aluminum-silicon or aluminum-silicon-copper.

PS CPI.EPI

FA AB; GI

MC CPI: L04-C06C; L04-C10C; L04-C10D; L04-C12

EPI: U11-C05D3; U11-D03B2

DRN 1694-U

L207 ANSWER 4 OF 4 WPIX (C) 2003 THOMSON DERWENT

AN 1998-335752 [30] WPIX

DNN N1998-262070 DNC C1998-104165

TI Planarised dual **damascene** metallisation - using copper line interconnection and selective CVD aluminium plug, etc., allowing use of copper interconnection for greater conductivity and less electromigration.

DC L03 U11

IN CHEN, F; CHEN, L; GUO, T; MOSELY, R C

PA (MATE-N) APPLIED MATERIALS INC

CYC 28

PI EP 851483 A2 19980701 (199830)\* EN 10p H01L021-768 <--  
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL  
PT RO SE SI

JP 10247650 A 19980914 (199847) 32p H01L021-3205 <--

SG 65719 A1 19990622 (199935) H01L021-768 <--

KR 98064795 A 19981007 (199949) H01L021-28 <--

TW 466737 A 20011201 (200252) H01L023-522

ADT EP 851483 A2 EP 1997-310668 19971230; JP 10247650 A JP 1997-370395  
19971226; SG 65719 A1 SG 1997-4692 19971226; KR 98064795 A KR  
1997-77841 19971230; TW 466737 A TW 1997-119967 19971230

PRAI US 1996-778205 19961230

IC ICM H01L021-28; H01L021-3205; H01L021-768; H01L023-522  
ICS H01L023-522

AB EP 851483 A UPAB: 19980730

A first conductive metal (18) is selectively deposited by **chemical vapour deposition (CVD)**

) to form a via plug (32). A barrier layer (20) is then deposited over the plug material and a layer of second metal formed by **physical vapour deposition** to fill the

**wire** definition (22). The second metal layer, barrier and dielectric layer (16) are then **planarised** to define a conductive **wire** (39). The first metal is Al deposited by the reaction of H<sub>2</sub> with (CH<sub>3</sub>)<sub>2</sub>Al, the barrier layer is Ti, Ta, or their nitrides, and the second metal is copper. **Planarisation** is by chemical mechanical **polishing**.

**USE** - The method is used for the metallisation of **semiconductor devices**.

**ADVANTAGE** - The process allows the use of copper interconnection for greater conductivity and less electromigration, integrated with an aluminium CVD process for filling small vias.

1A,B,C,D,E/3

FS CPI EPI

FA AB; GI

MC CPI: L03-H04E3

EPI: U11-C05C3; U11-C05C5; U11-C05D3; U11-D03B2

DRN 0352-U; 1532-U

=> d 1224 1-2 max

L224 ANSWER 1 OF 2 WPIX (C) 2003 THOMSON DERWENT

AN 2001-161595 [17] WPIX

DNN N2001-117880 DNC C2001-048379

TI Electromigration resistance enhancing structure of **semiconductor device** - includes barrier layer made of elements and different from elements comprising materials of first and second layers.

DC L03 U11

PA (FUIT) FUJITSU LTD

CYC 1

PI JP 11330001 A 19991130 (200117)\* 12p H01L021-28 <--

ADT JP 11330001 A JP 1998-139499 19980521

PRAI JP 1998-139499 19980521

IC ICM H01L021-28

ICS H01L021-3205

AB JP 11330001 A UPAB: 20010402

NOVELTY - Barrier layers (8-10) are provided between layers (2-4) and layers (5-7). The barrier layer is made of elements different from the elements in layers (2-4, 5-7).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor device** manufacturing method.

USE - For enhancing electromigration resistance in **semiconductor device**.

ADVANTAGE - By preventing diffusion of Cu from Cu embedding wiring layer or Cu plug, element characteristic durability of wiring layer and reliability of wiring layer structure are enhanced

DESCRIPTION OF DRAWING(S) - The figure shows the explanatory view of **semiconductor device**. (2-7) Layers;

(8-10) Barrier layer.

Dwg.1/8

FS CPI EPI

FA AB; GI

MC CPI: L04-C10H

EPI: U11-C05; U11-C05F

L224 ANSWER 2 OF 2 WPIX (C) 2003 THOMSON DERWENT

AN 1993-081993 [10] WPIX

TI Tungsten metallic wirings for silicon  
semiconductor device - deposited by plasma  
enhanced chemical vapour deposition on a  
tungsten nitride thin film.

AW ELECTROMIGRATION.

DC L03 U11

IN KIM, Y T; MIN, S

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TECHNOLOGY; (KOAD) KOREA ADV INST SCI & TECHNOLOGY

CYC 3

PI JP 05029317 A 19930205 (199310)\* 5p H01L021-3205 <--  
KR 9311538 B1 19931210 (199443) H01L021-285 <--  
US 5487923 A 19960130 (199611)B 7p C23C016-00 <--

ADT JP 05029317 A JP 1992-11118 19920124; KR 9311538 B1 KR 1991-12125  
19910716; US 5487923 A Cont of US 1992-912378 19920713, US  
1993-155915 19931123

PRAI KR 1991-12125 19910716

IC ICM C23C016-00; H01L021-285; H01L021-3205

AB US 5487923 A UPAB: 19960315 ABEQ treated as Basic

Forming a metallic wiring for a Si  
semiconductor device comprises: providing a Si  
semiconductor substrate; depositing a layer of W nitride on the  
substrate by a RF plasma enhanced CVD process which utilises a  
WF6-NH3-H2 reactant gas mixture and a 13.56 MHz glow discharge;  
depositing a layer of W on the layer of W nitride by a plasma  
enhanced CVD process which utilises a WF6-H2 reactant gas mixture  
and a 13.56 MHz glow discharge and produces F atoms from the WF6;  
wherein the W nitride layer prevents corrosion of the Si substrate  
by the F atoms during deposition of the W layer.

USE - Formation of metallic wirings in mfr.  
of highly integrated Si semiconductor elements.

ADVANTAGE - Corrosion of the Si substrate etc. by F atoms  
during the deposition of W, is prevented.

Dwg.1/3

FS CPI EPI

FA AB; GI

MC CPI: L04-C10A; L04-C12B

EPI: U11-C05C3; U11-C05C7; U11-C05D3

=> file hca

FILE 'HCA'

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L210 ANSWER 1 OF 6 HCA COPYRIGHT 2003 ACS

138:129793 Method and apparatus for fabrication of thin films by chemical vapor deposition. Paz De Araujo, Carlos A.; McMillan, Larry D.; Solayappan, Narayan; Bacon, Jeffrey W. (Symetrix Corporation, USA). U.S. US 6511718 B1 20030128, 26 pp., Cont.-in-part of U.S. 5,997,642. (English). CODEN: USXXAM. APPLICATION: US 1999-446226 19991217. PRIORITY: US 1997-892485 19970714; US 1997-971799 19971117; WO 1998-US14531 19980714.

AB The invention relates to methods for depositing high quality films of complex materials on substrates at high deposition rates, and app. for effecting such methods. Particularly, the invention relates to enhanced chem. vapor deposition from liq. sources of high quality thin films of a large variety of complex metal-oxide compds. at high deposition rates, and app. for effecting such methods. More particularly the invention relates to app. and methods for fabricating high quality thin films of ferroelec. layered superlattice materials. A venturi mist generator creates a mist comprising droplets having a mean diam. <1 .mu. from liq. precursors contg. multi-metal polyalkoxide compds. The mist is mixed and then passed into a gasifier where the mist droplets are gasified at a temp. of between 100.degree. and 250.degree., which is lower than the temp. at which the precursor compds. decomp. The gasified precursor compds. are transported by carrier gas through insulated tubing at ambient temp. to prevent both condensation and premature decompn. The gasified precursors are mixed with oxidant gas, and the gaseous reactant mixt. is injected through a shower head inlet into a deposition reactor in which a substrate is heated at a temp. of from 300.degree. to 600.degree.. The gasified precursors decomp. at the substrate and form a thin film of solid material on the substrate. The thin film is treated at elevated temps. of from 500.degree. to 900.degree. to form polycryst. metal oxide material, in particular, ferroelec. layered superlattice material.

IC ICM H05H001-24

ICS C23C016-40; C23C016-48; C23C016-56; B05D003-02; B05D001-34

NCL 427576000; 427584000; 427529000; 427255190; 427255320; 427255360; 427255250; 427422000; 427376200; 438758000

CC 76-3 (Electric Phenomena)

ST integrated circuit fabrication thin film chem  
vapor deposition

IT Ferroelectric materials

Films

Integrated circuits

Ion implantation

Rapid thermal annealing

(method and app. for fabrication of thin films by chem. vapor

deposition)  
IT 288389-40-2P, Barium bismuth **lead** niobium strontium  
**tantalum** oxide ((Ba,Pb,Sr)Bi<sub>2</sub>(Nb,Ta)2O<sub>9</sub>)  
(method and app. for fabrication of thin films by chem. vapor  
deposition)

L210 ANSWER 2 OF 6 HCA COPYRIGHT 2003 ACS  
134:246271 Completely encapsulated top electrode of a ferroelectric  
capacitor using a **lead-enhanced** encapsulation  
**layer**. Eastep, Brian Lee; Evans, Thomas A. (Ramtron  
International Corporation, USA). U.S. US 6211542 B1 20010403, 27  
pp., Cont.-in-part of U.S. 6,027,947. (English). CODEN: USXXAM.  
APPLICATION: US 1998-85280 19980527. PRIORITY: US 1996-700076  
19960820; US 1996-728740 19961011; US 1997-828157 19970327.

AB A ferroelec. capacitor includes a bottom electrode, a top electrode,  
and a ferroelec. layer located between the top and bottom electrodes  
that extends to completely encapsulate the top electrode, except for  
a contact hole to allow metalization of the top electrode. The  
total encapsulation of the top electrode reduces the sensitivity of  
the ferroelec. capacitor to hydrogen and thus improves elec.  
switching performance.

IT 11116-16-8, **Titanium nitride**  
(interconnect; encapsulated top electrode of a ferroelec.  
capacitor using a **lead-enhanced** encapsulation  
**layer** with reduced hydrogen sensitivity and improved  
elec. switching performance)

RN 11116-16-8 HCA

CN Titanium nitride (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	x	17778-88-0
Ti	x	7440-32-6

IC ICM H01L027-108  
ICS H01L029-76; H01L029-94; H01L031-119

NCL 257295000

CC 76-10 (Electric Phenomena)

ST ferroelec capacitor **lead enhanced** encapsulation  
**layer**

IT **Annealing**

Contact holes

Dielectric films

Encapsulation

Ferroelectric capacitors

Ferroelectric memory devices

Ferroelectric switching

**Integrated circuits**

Interconnections (electric)

(encapsulated top electrode of a ferroelec. capacitor using a  
**lead-enhanced** encapsulation **layer**)

- with reduced hydrogen sensitivity and improved elec. switching performance)
- IT Borophosphosilicate glasses  
(encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer**  
with reduced hydrogen sensitivity and improved elec. switching performance)
- IT Sputtering  
(etching, reactive; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT Machining  
(ion-beam milling; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT Coating process  
(metalization; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT Etching  
(sputter, reactive; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT 7440-32-6, Titanium, processes  
(adhesion layer, metal contacts; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT 12626-81-2, PZT 166877-45-8, Bismuth strontium **tantalum oxide**  
(ferroelec. film; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT 78-10-4, TEOS  
(glass; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT 11116-16-8, **Titanium nitride**  
(interconnect; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved elec. switching performance)
- IT 7429-90-5, Aluminum, processes  
(metal contacts; encapsulated top electrode of a ferroelec. capacitor using a **lead-enhanced encapsulation layer** with reduced hydrogen sensitivity and improved

- IT    elec. switching performance)  
 IT    75-73-0, Carbon tetrafluoride  
       (reactive ion etching; encapsulated top electrode of a ferroelec.  
       capacitor using a **lead-enhanced** encapsulation  
       **layer** with reduced hydrogen sensitivity and improved  
       elec. switching performance)  
 IT    7440-21-3, Silicon, processes  
       (substrate; encapsulated top electrode of a ferroelec. capacitor  
       using a **lead-enhanced** encapsulation  
       **layer** with reduced hydrogen sensitivity and improved  
       elec. switching performance)  
 IT    7440-06-4, Platinum, processes  
       (top and bottom electrode; encapsulated top electrode of a  
       ferroelec. capacitor using a **lead-enhanced**  
       encapsulation **layer** with reduced hydrogen sensitivity  
       and improved elec. switching performance)

L210 ANSWER 3 OF 6 HCA COPYRIGHT 2003 ACS

128:315683 Influence of overpolish time on the performance of W  
**Damascene** technology. Van Kranenburg, H.; Woerlee, P. H.  
 (MESA Research Institute, University of Twente, Enschede, 7500 AE,  
 Neth.). Journal of the Electrochemical Society, 145(4), 1285-1291  
 (English) 1998. CODEN: JESOAN. ISSN: 0013-4651.

Publisher: Electrochemical Society.

AB A metal-chem. mech. polishing (CMP) process for so-called inverse  
 metalization processes is described. The influence of a crit.  
 process parameter, overpolish time on pattern dependent erosion and  
 dishing for a 0.25 .mu.m W **Damascene** process, was studied.  
 Material removal rate and uniformity (WIWNU) were 150-250 nm/min and  
 3% (1 sigma), resp. Further the **pad** temp. close to the  
 contact area between **pad** and wafer indicates the end point  
 of polishing. Feature size and pattern d. effects on the CMP  
 performance are as expected. At proper rpm and pressure settings,  
 the effects are sufficiently small for application in  
**integrated circuit** processing. However,  
 surprisingly, with overpolishing erosion and dishing increase  
 rapidly, while at the end point the effects are negligible: 10%  
 overpolishing gave satisfactory results; 25% overpolishing was not  
 acceptable. Overpolishing of 10% was needed to obtain good (elec.)  
 yield (measured on meander-comb structures with pitch down to 0.8  
 .mu.m and length up to 3 m). The main dishing and erosion arise  
 after the end point of polishing. This is crucial for process  
 optimization and metal CMP modeling.

CC 76-3 (Electric Phenomena)

Section cross-reference(s): 66

ST overpolishing tungsten **Damascene** CMP

IT Polishing

(chem.-mech.; influence of overpolish time on performance of  
 tungsten **Damascene** technol.)

IT Electric conductors

(influence of overpolish time on performance of tungsten  
**Damascene** technol.)

- IT 7440-33-7, Tungsten, processes  
 (influence of overpolish time on performance of tungsten  
**Damascene technol.**)
- IT 206565-98-2, MSW 1000 206566-04-3, XJFW  
 (influence of overpolish time on performance of tungsten  
**Damascene technol.**)
- IT 1344-28-1, Alumina, uses 7722-84-1, Hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>), uses  
 7758-05-6, Potassium iodate  
 (slurry; influence of overpolish time on performance of tungsten  
**Damascene technol.**)

L210 ANSWER 4 OF 6 HCA COPYRIGHT 2003 ACS

125:209501 Growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures using a novel **iodine** doping source to achieve improved device performance at elevated temperatures. Maxey, C. D.; Jones, C. L.; Metcalfe, N. E.; Catchpole, R.; Houlton, M. R.; White, A. M.; Gordon, N. T.; Elliott, C. T. (GEC-Marconi Infra-Red Limited, Southampton, SO15 0EG, UK). Journal of Electronic Materials, 25(8), 1276-1285 (English) 1996. CODEN: JECMA5. ISSN: 0361-5235. Publisher: Minerals, Metals & Materials Society.

AB Band gap engineered Hg<sub>1-x</sub>CdxTe (MCT) heterostructures should lead to detectors with improved electro-optic and radiometric performance at elevated operating temps. Growth of such structures was accomplished using metalorg. vapor phase epitaxy (MOVPE). Acceptor doping with arsenic (As), using phenylarsine (PhAsH<sub>2</sub>), demonstrated 100% activation and reproducible control over a wide range of concns. (1 .times. 10<sup>15</sup> to 3.5 .times. 10<sup>17</sup> cm<sup>-3</sup>). Although vapor from elemental I showed the suitability of **iodine** as a donor in MCT, problems arose while controlling low donor concns. Initial studies using ethyliodide (EtI) demonstrated that this source could be used successfully to dope MCT, yielding the properties required for stable heterostructure devices, i.e., .apprx.100% activation, no memory problems and **low diffusion coeff.** Cryogenic alkyl cooling or very high diln. factors were required to achieve the concns. needed for donor doping below .apprxeq.10<sup>16</sup> cm<sup>-3</sup> due to the high vapor pressure of the alkyl. A study of an alternative org. **iodide** source, 2-methylpropyl iodide (2 MePrI), which has a much lower vapor pressure, improved control of low donor concns. 2 MePrI demonstrated the same donor source suitability as EtI and was used to control **iodine** concns. from .apprxeq.1 .times. 10<sup>15</sup> to 5 .times. 10<sup>17</sup> cm<sup>-3</sup>. The **iodine** from both sources only incorporated during the CdTe cycles of the interdiffused **multilayer** process (IMP) in a similar manner to both elemental **iodine** and As from PhAsH<sub>2</sub>. High resoln. secondary ion mass spectroscopy anal. showed that IMP scale modulations can still be identified after growth. The magnitude of these oscillations is consistent with a diffusion coeff. of .apprxeq.7 .times. 10<sup>-16</sup> cm<sup>2</sup>s<sup>-1</sup> for **iodine** in MCT at 365.degree.. Extrinsically doped device heterostructures, grown using 2 MePrI, have been intended to operate at elevated temps. either for long wavelength (8-12 .mu.m) equil. operation at 145 K or

nonequil. operation at 190 and 295 K in both the 3-5 .mu.m and 8-12 .mu.m wavelength ranges. Characterization of such device structures will be discussed. Linear arrays of mesa devices have been fabricated in these layers. Medium wave nonequil. device structures have demonstrated high quantum efficiencies and R<sub>OA</sub> = 37 .OMEGA.cm<sup>2</sup> for  $\lambda_{co} = 4.9 \text{ } \mu\text{m}$  at 190 K.

IT 7553-56-2, Iodine, uses  
(dopant; growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

RN 7553-56-2 HCA

CN Iodine (8CI, 9CI) (CA INDEX NAME)

I-I

IT 75-03-6, Ethyliodide  
(iodine dopant; growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

RN 75-03-6 HCA

CN Ethane, iodo- (8CI, 9CI) (CA INDEX NAME)

H<sub>3</sub>C—CH<sub>2</sub>—I

CC 76-3 (Electric Phenomena)

ST mercury cadmium telluride iodine doping; heterojunction mercury cadmium telluride

IT Semiconductor devices  
(heterojunction, growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

IT Epitaxy  
(metalorg. vapor-phase, growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

IT 822-65-1, Phenylarsine 7553-56-2, Iodine, uses  
(dopant; growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

IT 29870-72-2, Cadmium mercury telluride  
(heterostructure; growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

IT 75-03-6, Ethyliodide 513-38-2, 2-Methylpropyl iodide  
(iodine dopant; growth of fully doped Hg<sub>1-x</sub>CdxTe heterostructures by iodine doping for improved device performance at elevated temps.)

**semiconductor devices.** Misawa, Nobuhiro (Fujitsu Ltd, Japan). Jpn. Kokai Tokkyo Koho JP 06275612 A2 19940930 Heisei, 6 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1993-59889 19930319.

AB A flat Cu **wiring** (or contact) is manufd. by processes of forming a ditch opening in an insulating film formed on a substrate, depositing a thin barrier layer on the substrate including the area of the opening, depositing Cu layer thereon, removing the Cu and the barrier layers on the insulating film and forming the Cu **wiring** by removing part of the Cu layer in the opening so that its surface is below the level of the insulating film, forming a barrier layer by depositing the barrier material on the substrate and **polishing** the deposited barrier material by self-alignment method on the Cu **wiring** layer.

IT 25583-20-4, **Titanium nitride**  
(manuf. of Cu **wirings** and contacts in  
**semiconductor devices**)

RN 25583-20-4 HCA

CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)



IT 7553-56-2, **Iodine**, uses  
(manuf. of Cu **wirings** and contacts in  
**semiconductor devices** by **polishing**  
using)

RN 7553-56-2 HCA

CN Iodine (8CI, 9CI) (CA INDEX NAME)

I—I

IC ICM H01L021-3205  
ICS H01L021-28; H01L021-90; H05K003-02

CC 76-3 (Electric Phenomena)  
Section cross-reference(s): 75

ST copper **wiring** contact **semiconductor**  
device; titanium **nitride** barrier copper  
**wiring** contact

IT Electric contacts  
**Semiconductor devices**  
**Wire**

(manuf. of Cu **wirings** and contacts in  
**semiconductor devices**)

IT 7440-50-8, Copper, uses 7631-86-9, Silica, uses 25583-20-4  
, **Titanium nitride**  
(manuf. of Cu **wirings** and contacts in  
**semiconductor devices**)

IT 139566-53-3  
(manuf. of Cu **wirings** and contacts in

IT semiconductor devices by CVD using)  
 7553-56-2, Iodine, uses 7681-11-0, Potassium  
 iodide, uses  
 (manuf. of Cu wirings and contacts in  
 semiconductor devices by polishing  
 using)

L210 ANSWER 6 OF 6 HCA COPYRIGHT 2003 ACS

119:150365 Preparation of **bumps** for **semiconductor**

**devices**. Yamaguchi, Toshiyuki; Nosaka, Keiji (Fujitsu Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 04360537 A2 19921214 Heisei, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1991-136291 19910607.

AB The process includes the steps of: (a) laminating a metal interconnection (e.g., Al) and a **diffusion-preventing** metal layer (e.g., Ti) on a semiconductor layer; (b) forming an insulator layer on the whole surface and patterning the insulator layer to form an opening exposing the **laminate** of the metal interconnection and the **diffusion-preventing** metal layer; (c) successively forming a current-passing metal layer (e.g., Ti) and an adhesion-enhancing metal layer (e.g., Pt) and patterning the latter for removal from the area outside of a **bump**-forming region; (d) forming a resist layer and patterning it for removal from the **bump**-forming region to creat an opening; (e) electroplating a metal (e.g., Au) with the use of the current-passing metal layer to form a **bump** in the opening; and (f) removing the current-passing metal layer with the adhesion-enhancing metal layer as a mask.

IC ICM H01L021-321

CC 76-2 (Electric Phenomena)

ST **bump** prepn **semiconductor** device

IT Electrodes

(**bump**-, prepn. of, for **semiconductor** devices)

IT 7440-57-5P, Gold, uses

(**bumps**, prepn. of, for **semiconductor** devices)

IT 7440-06-4, Platinum, uses 7440-32-6, Titanium, uses

(in electroplating gold **bumps** for **semiconductor** devices)

IT 7429-90-5, Aluminum, uses

(interconnections, electroplating gold **bumps** for, in manuf. of **semiconductor** devices)

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L211 ANSWER 1 OF 10 HCA COPYRIGHT 2003 ACS

130:176255 Formation of dual **damascene** interconnections.

Chen, Liang-yuh; Tao, Rong; Guo, Ted; Mosely, Roderick Craig (Applied Materials, Inc., USA). PCT Int. Appl. WO 9909593 A1

**19990225**, 32 pp. DESIGNATED STATES: W: JP, KR, SG; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (English). CODEN: PIXXD2. APPLICATION: WO 1998-US17010 19980817. PRIORITY: US 1997-914521 19970819.

- AB The invention generally provides a metalization process for forming a highly integrated interconnect. More particularly, the invention provides a dual **damascene** interconnect module that incorporates a barrier layer deposited on all exposed surfaces of a dielec. layer which contains a dual **damascene** via and **wire** definition. A conductive metal is deposited on the barrier layer using .gtoreq.2 deposition methods to fill the via and **wire** definition prior to **planarization**.
- IT 7440-25-7, Tantalum, processes 12033-62-4  
, Tantalum nitride (TaN) 25583-20-4,  
Titanium nitride (TiN) 99039-55-1,  
Tantalum nitride silicide 121368-53-4,  
Silicon titanium nitride  
(metalization of dual **damascene** interconnections  
contg.)
- RN 7440-25-7 HCA
- CN Tantalum (8CI, 9CI) (CA INDEX NAME)

## Ta

- RN 12033-62-4 HCA
- CN Tantalum nitride (TaN) (6CI, 8CI, 9CI) (CA INDEX NAME)

## N≡ Ta

- RN 25583-20-4 HCA
- CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)



- RN 99039-55-1 HCA
- CN Tantalum nitride silicide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	x	17778-88-0
Ta	x	7440-25-7
Si	x	7440-21-3

- RN 121368-53-4 HCA
- CN Titanium nitride silicide (9CI) (CA INDEX NAME)

Component	Ratio	Component
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		Registry Number
N	x	17778-88-0
Ti	x	7440-32-6
Si	x	7440-21-3

IC ICM H01L021-768  
 CC 76-3 (Electric Phenomena)  
 ST dual **damascene** interconnection metalization  
 IT **Polishing**  
     (chem.-mech.; in metalization of dual **damascene**  
     interconnections)  
 IT **Vapor deposition process**  
     (chem.; in metalization of dual **damascene**  
     interconnections)  
 IT **Diffusion barrier**  
     (in dual **damascene** metalization)  
 IT Interconnections (electric)  
     (metalization of dual **damascene** interconnections)  
 IT **Integrated circuits**  
     (metalization of dual **damascene** interconnections for)  
 IT **Semiconductor device fabrication**  
     (metalization of dual **damascene** interconnections in)  
 IT Coating process  
     (metalization; dual **damascene** metalization)  
 IT **Vapor deposition process**  
     (phys.; in metalization of dual **damascene**  
     interconnections)  
 IT 1344-28-1, Alumina, processes 7429-90-5, Aluminum, processes  
     7440-21-3, Silicon, processes 7440-25-7, **Tantalum**  
     , processes 7440-32-6, Titanium, processes 7440-50-8, Copper,  
     processes 12033-62-4, **Tantalum nitride**  
     (TaN) 25583-20-4, **Titanium nitride**  
     (TiN) 37359-53-8, **Tungsten nitride**  
     99039-55-1, **Tantalum nitride silicide**  
     108729-83-5, **Tungsten nitride silicide**  
     121368-53-4, **Silicon titanium nitride**  
     (metalization of dual **damascene** interconnections  
     contg.)

L211 ANSWER 2 OF 10 HCA COPYRIGHT 2003 ACS

129:224515 **Semiconductor device**,  
**semiconductor memory device**, and their  
fabrication. Ishibashi, Hiroshi (Toshiba Corp., Japan). Jpn. Kokai  
Tokkyo Koho JP 10242147 A2 19980911 Heisei, 20 pp.  
(Japanese). CODEN: JKXXAF. APPLICATION: JP 1997-44247 19970227.

AB A **semiconductor device** and **semiconductor**  
**memory device** which are fabricated by a borderless contact  
technol. are described, including a **damascene** structure  
having a secure contact between **wiring** layers and their  
underlays. A recess is formed in an **interlayer** insulator  
film to expose its underlay, and the exposed underlay is selectively

etched to form a planar bottom to improve the film-formation properties of barrier and metal layers in the recess. Specifically, a plate electrode, which comprises Ru, Pt, Re, Os, Rh, Ir, Sr, W, Nb, Al, Ti, Ta, Mo, Cu, or Pb, of a **semiconductor** memory device may be formed in the recess.

IT 7440-25-7, **Tantalum**, uses  
(plate electrodes of **semiconductor** memory devices)

RN 7440-25-7 HCA

CN Tantalum (8CI, 9CI) (CA INDEX NAME)

Ta

IC ICM H01L021-3205

ICS H01L027-108; H01L021-8242

CC 76-3 (Electric Phenomena)

ST **semiconductor** memory device fabrication  
borderless contact

IT **Semiconductor** device fabrication  
(borderless contact formation in)

IT **Semiconductor** devices  
**Semiconductor** memory devices  
(borderless contacts in)

IT Electric contacts  
(borderless; in **semiconductor** device)

IT Etching  
(selective; in formation of borderless contacts in  
**semiconductor** device)

IT 7429-90-5, Aluminum, uses 7439-88-5, Iridium, uses 7439-92-1,  
**Lead**, uses 7439-98-7, Molybdenum, uses 7440-03-1,  
Niobium, uses 7440-04-2, Osmium, uses 7440-06-4, Platinum, uses  
7440-15-5, Rhenium, uses 7440-16-6, Rhodium, uses 7440-18-8,  
Ruthenium, uses 7440-24-6, Strontium, uses 7440-25-7,  
**Tantalum**, uses 7440-32-6, Titanium, uses 7440-33-7,  
Tungsten, uses 7440-50-8, Copper, uses  
(plate electrodes of **semiconductor** memory  
devices)

L211 ANSWER 3 OF 10 HCA COPYRIGHT 2003 ACS

129:88890 Forming fully **planarized** dual **damascene**

metallization using a copper line interconnect and a selective  
CVD aluminum plug. Chen, Liang-yuh; Guo, Ted; Mosely,  
Roderick Craig; Chen, Fusen (Applied Materials, Inc., USA). Eur.  
Pat. Appl. EP 851483 A2 19980701, 10 pp. DESIGNATED

STATES: R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE,  
MC, PT, IE, SI, LT, LV, FI, RO. (English). CODEN: EPXXDW.

APPLICATION: EP 1997-310668 19971230. PRIORITY: US 1996-778205  
19961230.

AB The invention provides a metallization process for forming a highly integrated interconnect. More particularly, the invention provides a dual **damascene** interconnect module that incorporates a

selective CVD Al via fill with a metal **wire**, preferably Cu, formed within a barrier layer. The invention provides the advantages of having Cu **wires** with lower resistivity and greater electromigration resistance than Al, a barrier layer between the Cu **wire** and the surrounding dielec. material, void-free, sub-half micron selective CVD Al via plugs, and a reduced no. of process steps to achieve such integration.

IT 7440-25-7, Tantalum, processes 12033-62-4  
, Tantalum nitride (TaN) 25583-20-4,  
Titanium nitride (TiN)  
(forming fully **planarized dual damascene**  
metalization using copper **wire** interconnect and  
selective CVD aluminum plug having barrier layer from)

RN 7440-25-7 HCA  
CN Tantalum (8CI, 9CI) (CA INDEX NAME)

Ta

RN 12033-62-4 HCA  
CN Tantalum nitride (TaN) (6CI, 8CI, 9CI) (CA INDEX NAME)

N≡ Ta

RN 25583-20-4 HCA  
CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)

N≡ Ti

IC ICM H01L021-768  
CC 76-2 (Electric Phenomena)  
ST **planarized dual damascene** metalization  
formation; **CVD** aluminum plug copper **wire**  
interconnection  
IT Interconnections (electric)  
(forming fully **planarized dual damascene**  
metalization using copper line interconnect and selective  
**CVD** aluminum plug)  
IT Integrated circuits  
(forming fully **planarized dual damascene**  
metalization using copper line interconnect and selective  
**CVD** aluminum plug for)  
IT Wires  
(forming fully **planarized dual damascene**  
metalization using copper **wire** interconnect and  
selective **CVD** aluminum plug)  
IT Diffusion barrier  
(forming fully **planarized dual damascene**

- metalization using copper **wire** interconnect and selective CVD aluminum plug having)
- IT Vapor deposition process  
 (selective; forming fully **planarized** dual **damascene** metalization using copper line interconnect and selective CVD aluminum plug)
- IT 7440-21-3, Silicon, processes  
 (doped; forming fully **planarized** dual **damascene** metalization using copper **wire** interconnect and selective CVD aluminum plug having barrier layer from)
- IT 7429-90-5, Aluminum, processes 7440-50-8, Copper, processes  
 (forming fully **planarized** dual **damascene** metalization using copper line interconnect and selective CVD aluminum plug)
- IT 1344-28-1, Aluminum oxide, processes 7440-25-7, Tantalum, processes 7440-32-6, Titanium, processes 12033-62-4, Tantalum nitride (TaN)  
 25583-20-4, Titanium nitride (TiN)  
 (forming fully **planarized** dual **damascene** metalization using copper **wire** interconnect and selective CVD aluminum plug having barrier layer from)

L211 ANSWER 4 OF 10 HCA COPYRIGHT 2003 ACS

126:194110 Manufacture of electrically conductive buried copper wiring layer for **semiconductor device** by **damascene** method. Okamoto, Shigeru (Fujitsu Ltd, Japan). Jpn. Kokai Tokkyo Koho JP 09022907 A2 19970121 Heisei, 10 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1995-169537 19950705.

AB The manuf. method involves (1) forming a concave domain in an insulating layer, (2) forming a barrier metal layer and a low O-concn. TiN layer, (3) depositing a Cu layer to bury the domain by CVD, and (4) selectively removing the metal, the TiN, and the Cu layer by chem.-mech. **polishing**. The **wiring** layer shows high electron-migration resistance and good barrier property. The manuf. using the low O-concn. TiN layer is effective for shortening incubation time in depositing the Cu layer. The barrier metal layer may be an amorphous Ti-Si-N layer obtained by heat-treating a deposited TiN layer in SiH<sub>4</sub>.

IT 121368-53-4, Titanium nitride silicide  
 (barrier metal layer, amorphous; manuf. of elec. conductive buried Cu **wiring** layer with electron-migration resistance by CVD)

RN 121368-53-4 HCA

CN Titanium nitride silicide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	x	17778-88-0
Ti	x	7440-32-6
Si	x	7440-21-3

IT 12033-62-4, Tantalum nitride  
 25583-20-4, Titanium nitride (TiN)  
 (barrier metal layer; manuf. of elec. conductive buried Cu  
 wiring layer with electron-migration resistance by  
 CVD)  
 RN 12033-62-4 HCA  
 CN Tantalum nitride (TaN) (6CI, 8CI, 9CI) (CA INDEX NAME)

N≡Ta

RN 25583-20-4 HCA  
 CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)

N≡  
Ti

IC ICM H01L021-3205  
 ICS H01L021-304  
 CC 76-3 (Electric Phenomena)  
 ST CVD copper wiring elec conductor; barrier metal  
 buried copper wiring; titanium nitride  
 elec conductive wiring; semiconductor  
 device buried copper wiring damascene  
 IT Semiconductor devices  
 (manuf. of elec. conductive buried Cu wiring layer with  
 electron-migration resistance by CVD)  
 IT 121368-53-4, Titanium nitride silicide  
 (barrier metal layer, amorphous; manuf. of elec. conductive  
 buried Cu wiring layer with electron-migration  
 resistance by CVD)  
 IT 1344-28-1, Alumina, uses 12033-62-4, Tantalum  
 nitride 25583-20-4, Titanium  
 nitride (TiN) 37359-53-8, Tungsten  
 nitride  
 (barrier metal layer; manuf. of elec. conductive buried Cu  
 wiring layer with electron-migration resistance by  
 CVD)  
 IT 7440-50-8, Copper, uses  
 (manuf. of elec. conductive buried Cu wiring layer with  
 electron-migration resistance by CVD)  
 IT 7803-62-5, Monosilane (SiH4), processes  
 (manuf. of elec. conductive buried Cu wiring layer with  
 electron-migration resistance by CVD)

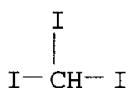
L211 ANSWER 5 OF 10 HCA COPYRIGHT 2003 ACS  
 121:262443 French limiting values for occupational exposure to  
 chemicals. Anon. (Fr.). Cahiers de Notes Documentaires, 153,  
 557-74 (French) 1993. CODEN: CNDIBJ. ISSN: 0007-9952.  
 AB Limit values (suggested limiting values and max. permissible values)

for occupational exposure to chems., including carcinogens, which have been published by the French Labor Ministry are presented in one table. This table is preceded by information on the following points: monitoring of workplace atmospheres (sampling and anal.; aerosols); permitted values (definitions and aims; additivity convention; elements and compds.; limiting occupational exposure values; carcinogens); mandatory values; and values recommended by the French National Health Insurance Fund (CNAM).

IT 75-47-8, Iodoform  
 (occupational exposure; occupational exposure and stds. for limiting workplace concns. of chems. in France)

RN 75-47-8 HCA

CN Methane, triiodo- (8CI, 9CI) (CA INDEX NAME)



CC 59-5 (Air Pollution and Industrial Hygiene)

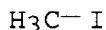
L211 ANSWER 6 OF 10 HCA COPYRIGHT 2003 ACS  
 107:154509 Coordination chemistry of methyl iodide. Burk, Mark J.; Segmuller, Brigitte; Crabtree, Robert H. (Sterling Chem. Lab., Yale Univ., New Haven, CT, 06520, USA). Organometallics, 6(10), 2241-6 (English) 1987. CODEN: ORGND7. ISSN: 0276-7333. OTHER SOURCES: CASREACT 107:154509.

AB Hydrogenation of  $[\text{Ir}(\text{COD})(\text{PPh}_3)_2]\text{SbF}_6$  (COD = cyclooctadiene) in the presence of MeI in  $\text{CH}_2\text{Cl}_2$  gave 85%  $[\text{IrH}_2(\text{IME})_2(\text{PPh}_3)_2]\text{SbF}_6$  (I) which contains two MeI groups coordinated via the iodine atoms. The Ir-I-C angles are 105.5 (4) and 108.2 (5).degree.. The coordinated MeI is activated toward nucleophilic attack at the carbon atom by  $\text{NEt}_3$ , the rate of which is enhanced 104-105-fold relative to free MeI. Removing the hydride ligands with  $\text{Me}_3\text{CCH}:\text{CH}_2$  leads to oxidative addn. to give  $[\text{MeIr}(\mu-\text{I})(\text{PPh}_3)_2]^2$  (II). Crystal structures of I and II were detd.

IT 74-88-4, Iodomethane, reactions  
 (hydrogenation of cyclooctadieniridium complex in presence of)

RN 74-88-4 HCA

CN Methane, iodo- (8CI, 9CI) (CA INDEX NAME)



CC 29-13 (Organometallic and Organometalloidal Compounds)  
 Section cross-reference(s): 75

IT 74-88-4, Iodomethane, reactions  
 (hydrogenation of cyclooctadieniridium complex in presence of)

L211 ANSWER 7 OF 10 HCA COPYRIGHT 2003 ACS  
 102:171148 Dry-etching process and its use. Druschke, Frank; Kraus,

Georg; Kuenzel, Ulrich; Ruh, Wolf Dieter; Schaefer, Rolf (IBM Deutschland G.m.b.H., Fed. Rep. Ger.; International Business Machines Corp.). Eur. Pat. Appl. EP 133621 A1 19850306, 15 pp. DESIGNATED STATES: R: DE, FR, GB. (German). CODEN: EPXXDW. APPLICATION: EP 1983-107604 19830802.

AB Cu is dry-etched near room temp. by glow discharge in Me or methylene compds., optionally mixed with H and/or inert gas at 40-200.degree., 0.0133-1.33 mbar, and high-frequency power of 0.5-4 W/cm<sup>2</sup> using plasma or chem. ion etching. The org. compds. are [H<sub>3</sub>Cl, CH<sub>3</sub>Br, **CH<sub>3</sub>I**, MeOH, acetone, dibutanediol, and diisomethane. The Cu, as a coating on glass, ceramic, or plastic, or masked with neg. and pos. masking resists, also polyimides, is etched selectively and used in manuf. of **printed circuit boards for lead wire** soldering, and thin-film magnet heads. For Me iodide, 0.04 mbar, 0.8 W/cm<sup>2</sup>, and 50.degree. are recommended. Thus, Cu vapor coating on plastic or glass substrate was etched by gaseous Me iodide at 20 cm<sup>3</sup>/min, 0.8 W/cm<sup>2</sup> of a 6 cm long high-frequency coil, and 50.degree. at a rate of 0.6 nm/s without redeposition or polymer degrdn.

IT **74-88-4, reactions**  
(copper etching with, elec. discharge for ion)

RN 74-88-4 HCA

CN Methane, iodo- (8CI, 9CI) (CA INDEX NAME)

### H<sub>3</sub>C—I

IC ICM H05K003-08  
ICS C23F001-00; H01L021-31  
CC 56-6 (Nonferrous Metals and Alloys)  
Section cross-reference(s): 76  
ST halide methyl etching copper; etching methyl iodide copper; ion etching methyl iodide copper; **printed circuit** copper ion etching  
IT Coating materials  
(vapor-deposited copper, dry etching of, in **printed circuit board** manuf.)  
IT **Electric circuits**  
(**printed**, copper etching for, by elec. discharge)  
IT 74-82-8D, halo derivs. **74-88-4, reactions**  
(copper etching with, elec. discharge for ion)

### L211 ANSWER 8 OF 10 HCA COPYRIGHT 2003 ACS

88:37925 Isocyanide insertion reactions. 1. The importance of .eta.-2-iminoacyl ligands as intermediates. Adams, Richard D.; Chodosh, Daniel F. (Dep. Chem., Yale Univ., New Haven, CT, USA). Journal of the American Chemical Society, 99(20), 6544-50 (English) 1977. CODEN: JACSAT. ISSN: 0002-7863.

AB The reaction of isocyanides (.eta.-5-C<sub>5</sub>H<sub>5</sub>)M(CO)<sub>3-x</sub>-(CNR)<sub>x</sub> (M = Mo, R = CH<sub>3</sub>, x = 1, 2; M = Mo, R = C<sub>6</sub>H<sub>5</sub>, x = 1; and M = W, R = CH<sub>3</sub>, x = 1) with MeI have been investigated. The products include the compds.

( $\eta_5\text{-C}_5\text{H}_5$ ) $\text{Mo}(\text{CO})_2$ ( $\eta_2\text{-CH}_3\text{CNCH}_3$ ) (I) and ( $\eta_5\text{-C}_5\text{H}_5$ ) $\text{Mo}(\text{CO})_2$ ( $\eta_2\text{-CH}_3\text{CNC}_6\text{H}_5$ ) (II), which contain novel dihapto iminoacyl ligands. Reaction of the tungsten anion produces the complex ( $\eta_5\text{-C}_5\text{H}_5$ ) $\text{W}(\text{CO})_2(\text{CNCH}_3)(\text{CH}_3)$ , in which the methyl group is attached to the tungsten atom. Complexes I and II readily add the ligands tetracyanoethylene, trimethyl phosphite, and triphenylphosphine to the metal atoms in a process that converts the  $\eta_2$ -iminoacyl group into an  $\eta_1$ -iminoacyl group. Addn. of iodide ion to I ultimately leads to formation of the complex ( $\eta_5\text{-C}_5\text{H}_5$ ) $\text{Mo}(\text{CO})_2$ (I) [ $\text{C}(\text{CH}_3)(\text{NHCH}_3)$ ], which contains a methyl(methylamino)carbene ligand. Reaction of the anion, ( $\eta_5\text{-C}_5\text{H}_5$ ) $\text{Mo}(\text{CO})(\text{CNCH}_3)_2^-$ , with methyl iodide produces the complex ( $\eta_5\text{-C}_5\text{H}_5$ ) $\text{Mo}(\text{CO})$ I[C]  
( $\text{N}(\text{CH}_3)_2\text{C}(\text{CH}_3)\text{N}(\text{CH}_3)$ ). This compd. was investigated by crystal structure anal. Attached to the molybdenum atom is a slightly skewed pentahapto cyclopentadienyl ring, a linear carbonyl group, and an iodine atom. The most interesting feature is a complex polyhapto carbon-nitrogen contg. ligand that has been interpreted as an iminodimethylaminocarbene. All the reaction products have been explained through a scheme that involves a uniform series of addns. and facile isocyanide insertion rearrangements.

- IT 74-88-4, reactions  
(reaction of, with molybdenum and tungsten isocyanide complexes)  
RN 74-88-4 HCA  
CN Methane, iodo- (8CI, 9CI) (CA INDEX NAME)

H<sub>3</sub>C-I

- CC 29-11 (Organometallic and Organometalloidal Compounds)  
Section cross-reference(s): 15  
IT 74-88-4, reactions  
(reaction of, with molybdenum and tungsten isocyanide complexes)

L211 ANSWER 9 OF 10 HCA COPYRIGHT 2003 ACS

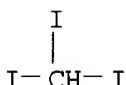
66:51655 Electrosynthesis of iodoform on a lead dioxide anode.

Dzhafarov, E. A.; Efendieva, Sh. M.; Bairamov, F. G.; Musaev, A. M. Azerbaidzhanskii Khimicheskii Zhurnal (4), 105-10 (Russian)  
1966. CODEN: AZKZAU. ISSN: 0005-2531.

- AB The effects of the soln. compn., the c.d., the temp., and the anodic material on the electrosynthesis of CHI<sub>3</sub> during electrolysis of solns. contg. KI (10-200 g./l.), EtOH (10-200 ml./l.), and Na<sub>2</sub>CO<sub>3</sub> (50-100 g./l.) were studied. The pH of the solns. was controlled by the passage of CO<sub>2</sub> into the soln. The cathodes were Pb and the anodes, PbO<sub>2</sub>, Pt, graphite, Ni, and stainless steel; a c.d. range of 5-60 amp./dm.<sup>2</sup> at 20-70.degree. was used. The distance between electrodes was 3.5 cm. With increase of temp. and of KI concn. and decrease of c.d., the current efficiency of CHI<sub>3</sub> formation increased. The best anodic material, in addn. to Pt, was PbO<sub>2</sub> which practically does not change during electrolysis. The optimum conditions were: electrolyte compn. KI 200 g., EtOH 200 ml., and Na<sub>2</sub>CO<sub>3</sub> 50-80 g./l.; c.d. 10-20 amp./dm.<sup>2</sup>; temp.

60.degree.; CHI<sub>3</sub> of 99.2-99.5% purity was obtained on PbO<sub>2</sub> anodes with current efficiency of 90%.

IT 75-47-8P  
 (formation of, on **lead** oxide (PbO<sub>2</sub>) anode)  
 RN 75-47-8 HCA  
 CN Methane, triiodo- (8CI, 9CI) (CA INDEX NAME)



CC 77 (Electrochemistry)  
 ST IODOFORM PREPN; **LEAD** DIOXIDE ANODES IODOFORM  
 IT Anodes  
 (lead oxide (PbO<sub>2</sub>), iodoform prep. at)  
 IT 75-47-8P  
 (formation of, on **lead** oxide (PbO<sub>2</sub>) anode)

L211 ANSWER 10 OF 10 HCA COPYRIGHT 2003 ACS  
 63:67793 Original Reference No. 63:12463d-f Use of photolytically induced surface reactions for the production of microcurrents.  
 White, P. Electronics Reliability Microminiaturization, 24, 161-6  
 From: CZ 1965(17), Abstr. 1891. (English) 1963.  
 AB Three methods are described: (1) A polymer insulating layer was produced by the influence of uv on the polymerization of butadiene (I) gas on metal surfaces. This layer can be utilized as a thin dielec. layer or as an acid-resistant mask for etching. The dependence of the film formation rate on time, pressure, and light intensity and the effects of O and H were investigated. By use of a I-He mixt. with a total pressure of 1 atm. and I partial pressure of 2 mm., the polymerization process did not have to be conducted in vacuum. (2) Metal was vaporized in the form of metal or org. compd. by CH free radicals produced by the photolytic decompn. of CH<sub>3</sub>I, CH<sub>3</sub>Br, or acetone vapor from vapor-deposited Sn or Pb layers. The dependence of the etching process on pressure and temp. was described. If the Sn film previous to the etching was exposed to O gas, etching started at higher temps. and more intense light action, because oxide films inhibited the elimination of metal by free radicals. (3) By photolytic decompn. of organometallic compds. (tetramethylgermanium), a metal film was formed. The area in which this reaction could take place was controlled by the wavelength and light intensity. This can be limited to 0.0005 in.  
 CC 9 (Electric and Magnetic Phenomena)  
 IT **Electric circuits**  
 (elec. insulators, metals and semiconductors for,  
 prep. by ultraviolet light)  
 IT 7439-92-1, **Lead**  
 (films of, for elec. microcircuits, ultraviolet-induced photolytic reactions in prep. of)

=> d 1222 1-2 cbib abs hitstr hitind

L222 ANSWER 1 OF 2 HCA COPYRIGHT 2003 ACS

131:331069 Chemical mechanical polishing slurries for interconnections and contacts. Grumbine, Steven K.; Streinz, Christopher C.; Mueller, Brian L. (Cabot Corporation, USA). U.S. US 5980775 A 19991109, 9 pp., Cont.-in-part of U.S. Ser. No. 753,482. (English). CODEN: USXXAM. APPLICATION: US 1997-827918 19970408. PRIORITY: US 1996-753482 19961126.

AB A chem. mech. polishing (CMP) compn. comprises an oxidizing agent (peroxides, e.g., 0.5-10 wt.% H<sub>2</sub>O<sub>2</sub>), a catalyst having multiple oxidn. states (e.g., 0.01-0.05 wt.% Fe(NO<sub>3</sub>)<sub>3</sub>), and a stabilizer (acids, nitriles, e.g., malonic acid), which is combined with an abrasive (e.g., 3-7 wt.% SiO<sub>2</sub>) or an abrasive pad to remove metal layers from a substrate. The CMP slurries are used to polish W and TiN based elec. interconnections or contacts in integrated circuits for semiconductor device fabrication.

IT 25583-20-4, Titanium nitride (TiN)  
(chem. mech. polishing slurries for interconnections and contacts)

RN 25583-20-4 HCA

CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)

N≡  
Ti

IC ICM C09K013-00

NCL 252079100

CC 76-3 (Electric Phenomena)

Section cross-reference(s): 49, 56, 67

ST chem mech polishing slurry integrated circuit

IT Abrasives

Catalysts

Electric contacts

Integrated circuits

Interconnections (electric)

Oxidizing agents

Semiconductor device fabrication

(chem. mech. polishing slurries for interconnections and contacts)

IT 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses

25583-20-4, Titanium nitride (TiN)

(chem. mech. polishing slurries for interconnections and contacts)

IT 7727-54-0, Ammonium persulfate 7758-05-6, Potassium iodate

16774-21-3, Diammonium cerium hexanitrate 37222-66-5, Oxone

(oxidants; chem. mech. polishing slurries for interconnections and contacts)

L222 ANSWER 2 OF 2 HCA COPYRIGHT 2003 ACS

123:45927 Manufacture of **semiconductor device**

involving dry etching of metal thin film. Tokashiki, Takeshi  
(Nippon Electric Co, Japan). Jpn. Kokai Tokkyo Koho JP 07094492 A2  
19950407 Heisei, 7 pp. (Japanese). CODEN: JKXXAF.

APPLICATION: JP 1994-55064 19940301. PRIORITY: JP 1993-175930  
19930624.

AB The manuf. involves dry etching of a noble metal thin film formed on a substrate to obtain a pattern by the following steps: (1) forming an etching mask pattern on the metal thin film, (2) dry etching the film in the presence of a halo-contg. gas contg. F, Cl, Br, and/or I, a .beta.-diketone which can form a metal complex with the noble metal, and a halo compd.-reducing gas. The noble metal may be Cu. Highly anisotropic etching with little side etching was carried out by the processes.

IT 7553-56-2, **Iodine**, processes

(etching gas; manuf. of **semiconductor device**  
involving plasma etching of **wiring** from noble  
**metal** thin film)

RN 7553-56-2 HCA

CN Iodine (8CI, 9CI) (CA INDEX NAME)

I—I

IT 25583-20-4, **Titanium nitride**

(etching mask; manuf. of **semiconductor device**  
involving plasma etching of **wiring** from noble  
**metal** thin film)

RN 25583-20-4 HCA

CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)

N≡  
Ti

IC ICM H01L021-3065

ICS H01L021-3205

CC 76-3 (Electric Phenomena)

ST **semiconductor device** etching dry metal; diketone  
beta etcng gas noble metal; anisotropic etching plasma  
**semiconductor device**; copper film etching dry  
diketone

IT Electric conductors

**Semiconductor devices**

(manuf. of **semiconductor device** involving  
plasma etching of **wiring** from noble **metal**  
thin film)

IT Group IB elements

(manuf. of **semiconductor device** involving  
plasma etching of **wiring** from noble **metal**  
thin film)

IT Sputtering  
 (etching, manuf. of **semiconductor device**  
 involving plasma etching of **wiring** from noble  
**metal** thin film)

IT Etching  
 (sputter, manuf. of **semiconductor device**  
 involving plasma etching of **wiring** from noble  
**metal** thin film)

IT 1522-22-1  
 (etching gas; manuf. of **semiconductor device**  
 involving plasma etching of **wiring** from noble  
**metal** thin film)

IT 7553-56-2, Iodine, processes 7664-41-7, Ammonia,  
 processes 7726-95-6, Bromine, processes 7782-41-4, Fluorine,  
 processes 7782-50-5, Chlorine, processes  
 (etching gas; manuf. of **semiconductor device**  
 involving plasma etching of **wiring** from noble  
**metal** thin film)

IT 12033-89-5, Silicon nitride, processes 25583-20-4,  
**Titanium nitride**  
 (etching mask; manuf. of **semiconductor device**  
 involving plasma etching of **wiring** from noble  
**metal** thin film)

IT 7440-06-4, Platinum, processes 7440-50-8, Copper, processes  
 (manuf. of **semiconductor device** involving  
 plasma etching of **wiring** from noble **metal**  
 thin film)

=> d his 1227-

FILE 'HCA'

L227 26 S (L4 OR L8) AND (L12 OR FILAMENT? OR RIBBON? OR STRAND?)  
 L228 21 S L227 NOT (L210 OR L211 OR L222)  
 L229 3 S L228 AND 1907-1999/PY

=> d 1229 1-3 cbib abs hitstr hitind

L229 ANSWER 1 OF 3 HCA COPYRIGHT 2003 ACS

136:176454 Compositions and structures for chemical mechanical polishing  
 of FERAM capacitors and method of fabricating FERAM capacitors using  
 same. Van Buskirk, Peter C.; Russell, Michael W.; Bilodeau, Steven  
 M.; Baum, Thomas H. (Advanced Technology Materials, Inc., USA).  
 U.S. US 6346741 B1 20020212, 16 pp., Cont.-in-part of U.S.  
 5,976,928. (English). CODEN: USXXAM. APPLICATION: US 1998-200499  
 19981125. PRIORITY: US 1997-975366 19971120.

AB An **integrated circuit** structures formed by chem.  
 mech. polishing (CMP) process, which comprises a conductive pathway  
 recessed in a dielec. substrate, wherein the conductive pathway  
 comprises conductive transmission lines encapsulated in a  
 transmission-enhancement material, and wherein the conductive

pathway is filled sequentially by a 1st layer of the transmission-enhancement material followed by the conductive transmission line; a 2nd **layer** of transmission-**enhancement** material encapsulating the conductive transmission line and contacting the 1st layer of the transmission-enhancement material, wherein the transmission-**enhancement** material is selected from the group consisting of high magnetic permeability material and high permittivity material. Such **integrated circuit** structure may comprise a device structure selected from the group consisting of capacitors, inductors, and resistors. Preferably, the transmission-**enhancement** material comprises Mg Mn ferrites, MgMnAl ferrites, Ba Sr titanate, **lead** Zr titanate, Ti oxide, Ta oxide, etc.

IC ICM H01L029-40  
 NCL 257664000  
 CC 76-3 (Electric Phenomena)  
 IT Electric coils  
     Encapsulation  
     Ferroelectric capacitors  
     Ferroelectric memory devices  
     **Integrated circuits**  
     Resistors  
       (compns. and structures for chem. mech. polishing of FERAM capacitors and method of fabricating FERAM capacitors using same)  
 IT 1314-61-0, **Tantalum** oxide 7429-90-5, Aluminum, processes 7440-33-7, Tungsten, processes 7440-50-8, Copper, processes 11099-19-7 13463-67-7, Titanium oxide, processes 37187-66-9, Magnesium manganese ferrite 37303-24-5, Barium strontium titanium oxide ((Ba,Sr)TiO<sub>3</sub>) 51680-22-9, Aluminum magnesium manganese ferrite 152060-61-2, **Lead** zirconium titanate  
       (compns. and structures for chem. mech. polishing of FERAM capacitors and method of fabricating FERAM capacitors using same)

L229 ANSWER 2 OF 3 HCA COPYRIGHT 2003 ACS

126:41425 Electric capacitor with high capacitance for semiconductor memory and its manufacture. Tani, Noriaki; Su, Koko; Suzuki, Ikuo; Ishikawa, Michio; Nakamura, Kyuzo (Ulvac Corp, Japan). Jpn. Kokai Tokkyo Koho JP 08250660 A2 19960927 Heisei, 6 pp.  
 (Japanese). CODEN: JKXXAF. APPLICATION: JP 1995-81897 19950314.

AB In the capacitor consisting of a substrate successively coated with a Pt lower electrode and an oxide dielec. thin film, the lower electrode film contains an interfacial additive which enhances the dielec. const. The additive may be Ru, Rh, Re, Os, and/or Ir. The manuf. is also claimed.  
 IC ICM H01L027-04  
     ICS H01L021-822  
 CC 76-10 (Electric Phenomena)  
 IT Capacitors  
     **Semiconductor memory devices**  
       (elec. capacitor with capacitance for semiconductor memory and its manuf.)  
 IT 7439-88-5, Iridium, uses 7440-04-2, Osmium, uses 7440-15-5,

Rhenium, uses 7440-16-6, Rhodium, uses 7440-18-8, Ruthenium, uses

(capacitance enhancer; elec. capacitor with capacitance for semiconductor memory and its manuf.)

IT 12047-27-7, Barium titanate, uses 12060-00-3, Lead titanate 12060-59-2, Strontium titanate 12430-73-8, Barium strontium titanium oxide (BaSrTi<sub>2</sub>O<sub>6</sub>) 50811-07-9, Bismuth strontium tantalum oxide (Bi<sub>2</sub>SrTa<sub>2</sub>O<sub>9</sub>) 111242-35-4, Lead titanium zirconium oxide (PbTi<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>3</sub>) 184579-52-0, Lanthanum lead titanium zirconium oxide (La<sub>0.1</sub>Pb<sub>0.9</sub>Ti<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>3</sub>) (elec. capacitor with capacitance for semiconductor memory and its manuf.)

L229 ANSWER 3 OF 3 HCA COPYRIGHT 2003 ACS

111:206670 A new twin-well CMOS process using nitridized-oxide-LOCOS (NOLOCOS) isolation technology. Tsai, Hong Hsiang; Yu, Chin Lin; Wu, Ching Yuan (Inst. Electron., Natl. Chiao-Tung Univ., Hsinchu, Taiwan). IEEE Electron Device Letters, 10(7), 307-9 (English) 1989. CODEN: EDLEDZ. ISSN: 0741-3106.

AB A twin-well CMOS process using the nitridized pad-oxide film as a buffer layer for the enhanced local oxidn. of silicon (LOCOS) has been developed in which the nitridized pad oxide is used to obtain a defect-free and near-zero bird's beak field isolation structure. The principal feature of the developed novel process is that high-temp. nitridation of thin pad oxide is simultaneously used to increase the junction depth of the As-implanted n-well. Both n- and p-channel MOSFET's fabricated by the developed twin-well CMOS process have been characterized and compared with those fabricated by the conventional LOCOS isolation technique.

CC 76-3 (Electric Phenomena)

IT Semiconductor devices

(in quantum well complimentary MOS, nitridation and local oxidn. of silicon technol. in fabrication of)

IT 14280-20-7, Boron(2+), uses and miscellaneous (redn. of lateral diffusion of impurities in MOS FET obtained by implantation with)

=> d his 1230-

FILE 'HCA'

L230 49 S (L4 OR L8) AND (L12 OR FILAMENT? OR RIBBON? OR STRAND?)  
 L231 38 S L230 NOT (L210 OR L211 OR L222 OR L229)  
 L232 9 S L231 AND 1907-1999/PY

=> d 1232 1-9 cbib abs hitstr hitind

L232 ANSWER 1 OF 9 HCA COPYRIGHT 2003 ACS

135:115642 Semiconductor devices with good stability and a flat insulating layer with a dopant. Watanabe, Hiroyuki; Mizuhara, Hideki; Misawa, Kaori; Hirase, Masaki; Aoe, Hiroyuki

(Sanyo Electric Co., Ltd., Japan). U.S. US 6268657 B1 20010731, 48 pp., Cont.-in-part of U.S. 6,214,479. (English). CODEN: USXXAM. APPLICATION: US 1997-877931 19970618. PRIORITY: US 1995-528123 19950914; JP 1996-181593 19960620; US 1997-949283 19971021.

- AB A **semiconductor device** and a process for producing the same. The device has two conducting layers that are spaced from each other and an insulating film for elec. insulating these two conducting layers from each other. The insulating film contains contact holes with plugs being embedded therein so as to elec. connect these two conducting layers by the plugs. The process contains a step of forming the insulating film on the lower conducting layer. An impurity having a kinetic energy is introduced into the insulating film. Next, contact holes are formed in the insulating film, and then plugs are formed in the contact holes. An upper conducting layer is formed on the insulating film so as to be elec. connected to the plugs.
- IT 7440-25-7, **Tantalum**, uses 7553-56-2,  
**Iodine**, uses  
     (**semiconductor devices** with good stability  
     and flat insulating layer with dopant)
- RN 7440-25-7 HCA
- CN Tantalum (8CI, 9CI) (CA INDEX NAME)

## Ta

- RN 7553-56-2 HCA
- CN Iodine (8CI, 9CI) (CA INDEX NAME)

## I-I

- IC ICM H01L021-321  
     ICS H01L023-485
- NCL 257759000
- CC 76-3 (Electric Phenomena)
- ST doping dielec film **semiconductor device**
- IT Films  
     (elec. conductive; **semiconductor devices** with  
     good stability and flat insulating layer with dopant)
- IT Electric conductors  
     (films; **semiconductor devices** with good  
     stability and flat insulating layer with dopant)
- IT Noble gases, processes  
     (ions; **semiconductor devices** with good  
     stability and flat insulating layer with dopant)
- IT Contact holes  
     Dielectric films  
     Dopants  
     Doping  
     Ion implantation  
     **Semiconductor devices**

(semiconductor devices with good stability  
and flat insulating layer with dopant)

IT Polymers, processes  
(semiconductor devices with good stability  
and flat insulating layer with dopant)

IT Group IIIB elements  
Group IVA elements  
Group IVB elements  
Group VA elements  
Group VB elements  
Group VIB elements  
Group VIIIB elements  
Noble gases, uses  
(semiconductor devices with good stability  
and flat insulating layer with dopant)

IT 7440-21-3, Silicon, processes 7440-33-7, Tungsten, processes  
(semiconductor devices with good stability  
and flat insulating layer with dopant)

IT 7429-90-5, Aluminum, uses 7439-90-9, Krypton, uses 7439-92-1,  
Lead, uses 7440-01-9, Neon, uses 7440-03-1, Niobium,  
uses 7440-25-7, Tantalum, uses 7440-31-5, Tin,  
uses 7440-32-6, Titanium, uses 7440-36-0, Antimony, uses  
7440-37-1, Argon, uses 7440-38-2, Arsenic, uses 7440-42-8,  
Boron, uses 7440-55-3, Gallium, uses 7440-56-4, Germanium, uses  
7440-58-6, Hafnium, uses 7440-59-7, Helium, uses 7440-62-2,  
Vanadium, uses 7440-63-3, Xenon, uses 7440-69-9, Bismuth, uses  
7440-74-6, Indium, uses 7553-56-2, Iodine, uses  
7704-34-9, Sulfur, uses 7726-95-6, Bromine, uses 7727-37-9,  
Nitrogen, uses 7782-44-7, Oxygen, uses 7782-49-2, Selenium, uses  
7782-50-5, Chlorine, uses 10043-92-2, Radon, uses 13494-80-9,  
Tellurium, uses  
(semiconductor devices with good stability  
and flat insulating layer with dopant)

L232 ANSWER 2 OF 9 HCA COPYRIGHT 2003 ACS

132:68719 Variation of 66 elements in European bottled mineral waters.

Misund, A.; Frengstad, B.; Siewers, U.; Reimann, C. (Geological Survey of Norway, Trondheim, N-7491, Norway). Science of the Total Environment, 243/244, 21-41 (English) 1999. CODEN:

STENDL. ISSN: 0048-9697. Publisher: Elsevier Science Ireland Ltd..

AB Fifty-six bottled mineral waters bought at random all over Europe were analyzed for 66 chem. elements by ICP-AES, ICP-MS and IC-techniques. Results show that there is a wide spread in the chem. compn. of mineral waters. The EEC drinking water safeguard values for chem. constituents do not apply to mineral water, although mineral water is increasingly used for general drinking water purposes. Only 15 of the randomly selected 56 mineral waters would fulfil the drinking water regulations for all parameters where action levels are defined. Differences in chem. compn. obsd. between countries or regions are due to geol. environment and to different taste or local regulations of what is mineral water. There are indications that element concns. for some

unwanted constituents (e.g. Pb) are higher in waters sold in glass bottles than in those in plastic bottles. Some elements show a clear regional dependency. Studying the large natural variation in concn. for many of the 66 studied elements it becomes clear that we know little about the natural variation of element concn. in water and the health effects of most elements in drinking water.

IT 7440-25-7, Tantalum, miscellaneous  
 7553-56-2, Iodine, miscellaneous  
 (variation of 66 elements in European bottled mineral waters)  
 RN 7440-25-7 HCA  
 CN Tantalum (8CI, 9CI) (CA INDEX NAME)

Ta

RN 7553-56-2 HCA  
 CN Iodine (8CI, 9CI) (CA INDEX NAME)

I-I

CC 61-1 (Water)

L232 ANSWER 3 OF 9 HCA COPYRIGHT 2003 ACS

131:215158 Inorganic lubricant-coated glass fiber **strands** and products including the same. Novich, Bruce E.; Robertson, Walter J.; Velpari, Vedagiri; Wu, Xiang (PPG Industries Ohio, Inc., USA). PCT Int. Appl. WO 9944960 A1 19990910, 80 pp. DESIGNATED

STATES: W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG. (English). CODEN: PIXXD2. APPLICATION: WO 1999-US4087 19990225. PRIORITY: US 1998-34525 19980303; US 1998-170780 19981013.

AB A coated fiber **strand** comprises at least one glass fiber having a primary layer of a dried residue of an aq. sizing compn. applied to at least a portion of a surface of the fiber, the aq. sizing compn. comprising: (a) non-hydratable, lamellar, inorg. solid lubricant particles having a hardness value which does not exceed the hardness value of the glass fiber; and (b) a polymeric material, the aq. sizing compn. being essentially free of glass materials.

IC ICM C03C025-02  
 ICS C08J005-08; H05K001-03  
 CC 37-6 (Plastics Manufacture and Processing)  
 IT Epoxy resins, uses  
 (acrylates; inorg. lubricant-coated glass fiber **strands** and products including the same)  
 IT Printed circuit boards

## Sizing

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Glass fibers, processes

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Acrylic polymers, uses

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Aminoplasts

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Epoxy resins, uses

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Phenolic resins, uses

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Polyamides, uses

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Polyesters, uses

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Polyolefins

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Reinforced plastics

(inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Polyurethanes, uses

(thermoplastic; inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Plastics, uses

(thermoplastics; inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Plastics, uses

Polyurethanes, uses  
(thermosetting; inorg. lubricant-coated glass fiber **strands** and products including the same)

IT Polyesters, uses

(unsatd.; inorg. lubricant-coated glass fiber **strands** and products including the same)

IT 1317-33-5, Molybdenum disulfide, uses 7782-42-5, Graphite, uses

7790-80-9, Cadmium iodide 9003-39-8, Polyvinyl

pyrrolidone 9005-25-8, Starch, uses 9036-19-5, IGEPAL CA-630

10043-11-5, Boron nitride, uses 12039-55-3, Tantalum

diseLENide 12058-18-3, MolybdenumdiseLENide 12067-46-8, Tungsten

diseLENide 12138-09-9, Tungsten disulfide 12143-72-5,

Tantalum disulfide 12624-35-0, VERSAMID 140 21548-73-2,

Silver sulfide 24937-05-1, DESMOPHEN 2000 25068-38-6, EPON 826

106392-12-5, PLURONIC F-108 217478-86-9, RD-847A 241811-13-2,

## Epi-Rez 3522W66

(inorg. lubricant-coated glass fiber **strands** and products including the same)

L232 ANSWER 4 OF 9 HCA COPYRIGHT 2003 ACS

130:46281 Amine fluoride process gas and dry etching and cleaning using it. Iwamori, Akira; Fukuda, Noboru; Nozaki, Shohei; Nakajima, Yasuo (Mitsui Chemicals Inc., Japan). Jpn. Kokai Tokkyo Koho JP 10303181 A2 19981113 Heisei, 7 pp. (Japanese). CODEN: JKXXAF.

APPLICATION: JP 1997-111345 19970428.

AB The process gas contains an amine fluoride. The dry etching or cleaning of silicon oxide, carbide, nitride, or a metal (compd.) is carried out by using the above gas and optionally halogen (compds.). The method is also applicable for chambers in the presence elec. discharge or under heating. The process gas is milder to the environment and capable of fine processing to be useful for manuf. of **semiconductor integrated circuits** and liq.-crystal displays, etc.

IT 7440-25-7, Tantalum, processes 12033-62-4  
, Tantalum nitride 25583-20-4,  
**Titanium nitride**

(dry etching and cleaning with amine fluoride process gas)

RN 7440-25-7 HCA

CN Tantalum (8CI, 9CI) (CA INDEX NAME)

Ta

RN 12033-62-4 HCA

CN Tantalum nitride (TaN) (6CI, 8CI, 9CI) (CA INDEX NAME)

N≡ Ta

RN 25583-20-4 HCA

CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)



IT 7553-56-2, Iodine, uses  
(dry etching and cleaning with amine fluoride process gas)

RN 7553-56-2 HCA

CN Iodine (8CI, 9CI) (CA INDEX NAME)

I-I

IC ICM H01L021-3065

ICS C23F004-00; H01L021-304

CC 76-3 (Electric Phenomena)

IT Bromides, uses  
Chlorides, uses  
**Iodides, uses**  
(dry etching and cleaning with amine fluoride process gas)  
IT 409-21-2, Silicon carbide, processes 1299-86-1, Aluminum carbide  
1302-81-4, Aluminum sulfide 1310-53-8, Germanium oxide, processes  
1312-43-2, Indium oxide 1313-99-1, Nickel oxide, processes  
1314-13-2, Zinc oxide, processes 1314-23-4, Zirconium oxide,  
processes 1314-35-8, Tungsten oxide, processes 1314-61-0,  
**Tantalum** oxide 1314-87-0, **Lead** sulfide  
1314-98-3, Zinc sulfide, processes 1317-33-5, Molybdenum sulfide  
(MoS<sub>2</sub>), processes 1332-29-2, Tin oxide 1332-37-2, Iron oxide,  
processes 1335-25-7, **Lead** oxide 1344-28-1, Aluminum  
oxide, processes 1344-70-3, Copper oxide 7429-90-5, Aluminum,  
processes 7439-88-5, Iridium, processes 7439-89-6, Iron,  
processes 7439-92-1, **Lead**, processes 7439-96-5,  
Manganese, processes 7439-98-7, Molybdenum, processes 7440-02-0,  
Nickel, processes 7440-21-3, Silicon, processes 7440-22-4,  
**Silver**, processes 7440-25-7, **Tantalum**, processes  
7440-31-5, Tin, processes 7440-32-6, Titanium, processes  
7440-33-7, Tungsten, processes 7440-47-3, Chromium, processes  
7440-48-4, Cobalt, processes 7440-50-8, Copper, processes  
7440-56-4, Germanium, processes 7440-62-2, Vanadium, processes  
7440-66-6, Zinc, processes 7440-67-7, Zirconium, processes  
7440-74-6, Indium, processes 7631-86-9, Silica, processes  
11098-99-0, Molybdenum oxide 11099-11-9, Vanadium oxide  
11104-61-3, Cobalt oxide 11104-62-4, Cobalt silicide 11104-85-1,  
Molybdenum silicide 11113-75-0, Nickel sulfide 11115-78-9,  
Copper sulfide 11118-57-3, Chromium oxide 11126-12-8, Iron  
sulfide 11129-43-4, Iridium silicide 11129-60-5, Manganese oxide  
11130-24-8, Vanadium sulfide 11130-49-7, Chromium carbide  
11148-21-3 12033-62-4, **Tantalum nitride**  
12033-89-5, Silicon nitride, processes 12039-13-3, Titanium  
sulfide (TiS<sub>2</sub>) 12040-52-7, Silver carbide 12070-06-3,  
**Tantalum** carbide 12070-08-5, Titanium carbide  
12070-10-9, Vanadium carbide 12070-12-1, Tungsten carbide  
12070-14-3, Zirconium carbide 12138-09-9, Tungsten sulfide  
12623-97-1, Chromium sulfide 12626-44-7, Chromium silicide  
12626-76-5, Iron silicide 12626-89-0, Manganese silicide  
12627-41-7, Tungsten silicide 12627-57-5, Molybdenum carbide  
12640-64-1, Iron carbide 12643-20-8, Copper silicide 12645-46-4,  
Iridium oxide 12646-17-2, Manganese nitride 12653-56-4, Cobalt  
sulfide 12674-04-3, Vanadium nitride 12687-82-0, Manganese  
sulfide 12705-37-2, Chromium nitride 12710-36-0, Nickel carbide  
12737-58-5, Germanium sulfide 12738-11-3, Nickel nitride  
12738-87-3, Tin sulfide 12738-91-9, Titanium silicide  
12777-96-7, Manganese carbide 13463-67-7, Titanium oxide,  
processes 20667-12-3, Silver oxide 20737-02-4, Silver nitride  
(Ag<sub>3</sub>N) 21548-73-2, Silver sulfide (Ag<sub>2</sub>S) 24304-00-5, Aluminum  
nitride 25583-20-4, **Titanium nitride**  
25617-98-5, Indium nitride 25658-42-8, Zirconium nitride  
37189-51-8, Zirconium silicide 37231-03-1, Indium sulfide

37244-09-0, Zirconium sulfide 37245-77-5, Iron nitride  
 37245-81-1, Molybdenum nitride 37359-53-8, **Tungsten**  
**nitride** 39300-69-1, **Lead** carbide 39467-10-2,  
 Nickel silicide 51177-04-9, Cobalt carbide 51680-36-5, Copper  
 carbide 51845-89-7, Germanium nitride 51845-91-1, Iridium  
 carbide 52036-89-2, **Lead** nitride 52036-93-8, Tin  
 carbide 52037-56-6, Vanadium silicide 52489-06-2, Silver  
 silicide 52934-19-7, Iridium sulfide 52953-72-7,  
**Tantalum** silicide 55326-68-6, Cobalt nitride 55574-97-5,  
 Tin nitride 67527-63-3, Germanium carbide 68247-39-2, Indium  
 silicide 69255-78-3 74499-90-4, Zinc carbide 96777-69-4,  
 Copper nitride 98285-50-8, Indium carbide 103289-29-8, Tin  
 silicide 106698-75-3, Aluminum silicide 111446-69-6,  
**Tantalum** sulfide 128579-03-3, Zinc nitride 128579-24-8,  
 Zinc silicide 205307-78-4, Iridium nitride  
 (dry etching and cleaning with amine fluoride process gas)

IT 335-01-3, Trifluoromethylidifluoroamine 359-62-6,  
 Bis(trifluoromethyl)fluoroamine 432-03-1,  
 Tris(trifluoromethyl)amine **7553-56-2, Iodine**,  
 uses 7726-95-6, Bromine, uses 7782-50-5, Chlorine, uses  
 (dry etching and cleaning with amine fluoride process gas)

L232 ANSWER 5 OF 9 HCA COPYRIGHT 2003 ACS

125:182896 Experimental studies of laser-created plasma as a source of highly charged ions. Mroz, W.; Parys, P.; Wolowski, J.; Woryna, E.; Laska, L.; Masek, K.; Rohlena, K.; Collier, J.; Haseroth, H.; et al. (Institute of Optoelectronics, Military University of Technology, Warsaw, 01-489, Russia). AIP Conference Proceedings, 369(Pt. 2, Laser Interaction and Related Plasma Phenomena, Pt. 2), 1029-1034 (English) 1996. CODEN: APCPCS. ISSN: 0094-243X.

Publisher: AIP Press.

AB The main results of exptl. studies on multiply charged ions generated from a laser-produced plasma and registered at large distances from targets are presented. The results were achieved using laser systems with different fundamental wavelengths,  $\lambda$ , energies, EL, and laser pulse lengths,  $\tau$ : CO<sub>2</sub> lasers, CERN: EL.apprx.50 J,  $\tau$ .apprx.70 ns, Troitsk Institute for Innovative and Thermonuclear Investigations, EL.apprx.100 J,  $\tau$ .apprx.2.5 ns and 25 ns; Nd:glass laser, Institute of Plasma Physics and Laser Microfusion: EL.ltoreq.20 J,  $\tau$ .apprx.1 ns; Iodine laser PERUN, Institute of Physics, Academy of Sciences of the Czech Republic: EL .ltoreq. 50 J,  $\tau$ .apprx.350 ps. Al, Cu, Fe, Mo, **Ta**, Pt, and Pb were used as target materials. The principal ion diagnostics for measuring ion charge states and energy distributions were based on the time-of-flight method: ion collectors (IC) and ion energy analyzers (IEA). In a few expts., Thomson parabola ion spectrograph (TS) was used. Up-to-date max. measured charge state of **Ta** ions was z=53 and max. ion energy was Ei=4.8 MeV.

IT **7440-25-7D, Tantalum**, ions, properties  
 (laser-created plasma as a source of highly charged ions)

RN 7440-25-7 HCA

CN Tantalum (8CI, 9CI) (CA INDEX NAME)

Ta

CC 76-11 (Electric Phenomena)

IT 7429-90-5D, Aluminum, ions, properties 7439-89-6D, Iron, ions, properties 7439-92-1D, Lead, ions, properties 7439-98-7D, Molybdenum, ions, properties 7440-06-4D, Platinum, ions, properties 7440-25-7D, **Tantalum**, ions, properties 7440-50-8D, Copper, ions, properties (laser-created plasma as a source of highly charged ions)

L232 ANSWER 6 OF 9 HCA COPYRIGHT 2003 ACS

119:215374 Potting compositions for **integrated circuit** packages. Yamanaka, Toshiro (Nippon Electric Glass Co, Japan). Jpn. Kokai Tokkyo Koho JP 05147974 A2 19930615 Heisei, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1991-336141 19911125.

AB The potting compns. comprise (1) 45-90 vol.% low-m.p. amorphous or cryst. glass contg. Ag<sub>2</sub>O and/or silver halide 15-85, P<sub>2</sub>O<sub>5</sub>, GeO<sub>2</sub>, WO<sub>3</sub>, and/or MoO<sub>3</sub> 5-50, oxide or halide of Pb, Ba, Sr, Ca, Zn, Cu, Mn, and bi 0-40, and TiO<sub>2</sub>, V<sub>2</sub>O<sub>5</sub>, B<sub>2</sub>O<sub>3</sub>, N<sub>2</sub>O<sub>5</sub>, Ta<sub>2</sub>O<sub>5</sub>, Fe<sub>2</sub>O<sub>3</sub>, SiO<sub>3</sub>, and/or Al<sub>2</sub>O<sub>3</sub> 0-25 mol% and (2) 10-55 vol.% refractory powder. The potting compns. do not contain poisonous materials and can be used for **integrated circuit** packages at <330.degree..

IC ICM C03C008-24

CC 76-2 (Electric Phenomena)

ST Section cross-reference(s): 57

IT **integrated circuit** potting compn; glass  
refracetory potting compn

IT Potting compositions

(contg. amorphous glass and refractory powder for  
**integrated circuits**)

IT **Electric circuits**

(**integrated**, potting compns. for, contg. amorphous  
glass and refractory powder)

IT Glass, oxide

(soft, potting compns. contg. refractory powder and, for  
**integrated circuits**)

IT 1310-53-8, Germania, uses 1314-13-2, Zinc oxide, uses 1314-56-3,  
Phosphorus pentoxide, uses 1317-36-8, Lead oxide, uses  
1317-38-0, Cupric oxide, uses 7446-07-3, Tellurium oxide (TeO<sub>2</sub>)  
7783-49-5, Zinc fluoride 7783-96-2, Silver **iodide**  
20667-12-3, Silver oxide (Ag<sub>2</sub>O)

(amorphous glass contg., potting compns. contg. refractory powder  
and, for **integrated circuits**)

IT 1303-86-2, Boria, uses 1309-37-1, Ferric oxide, uses 1313-27-5,  
Molybdenum trioxide, uses 1313-96-8, Niobium pentoxide  
1314-35-8, Tungsten trioxide, uses 1314-61-0, **Tantalum**  
pentoxide 1314-62-1, Vanadium pentoxide, uses 1344-28-1,  
Alumina, uses 7631-86-9, Silica, uses

(glass contg., potting compns. contg. refractory powder and, for integrated circuits)

- IT 12060-00-3, Lead titanate 14940-68-2, Zircon  
 62585-91-5 112003-81-3, Calcium lead titanium oxide  
 (Ca0.3Pb0.7TiO<sub>3</sub>)  
 (powd., potting compns. contg. low-m.p. glass and, for integrated circuits)
- IT 1302-65-4, Eucryptite  
 (.beta.-, powd., potting compns. contg. low-m.p. glass and, for integrated circuits)

L232 ANSWER 7 OF 9 HCA COPYRIGHT 2003 ACS

118:207041 Development of frozen whale blubber and liver reference materials for the measurement of organic and inorganic contaminants. Wise, Stephen A.; Schantz, Michele M.; Koster, Barbara J.; Demiralp, Rabia; Mackey, Elizabeth A.; Greenberg, Robert R.; Burow, Mechthild; Ostapczuk, Peter; Lillestolen, Ted I. (Chem. Sci. Tecnol. Lab., Natl. Inst. Stand. Technol., Gaithersburg, MD, 20899, USA). Fresenius' Journal of Analytical Chemistry, 345(2-4), 270-7 (English) 1993. CODEN: FJACES. ISSN: 0937-0633.

AB Fresh frozen homogenates of pilot whale blubber and liver tissue were prep'd. for use as control materials for the detn. of org. and inorg. contaminants in marine mammal tissue analyses. The blubber material was analyzed to det. 30 polychlorinated biphenyl congeners and 16 chlorinated pesticides using gas chromatog. with electron capture detection and gas chromatog.-mass spectrometry. A total of 39 trace elements and methylmercury were detd. in the liver homogenate using instrumental neutron activation anal., voltammetry, and cold vapor at. absorption spectroscopy. The prepn. and anal. of these 2 tissue materials are part of the development of marine mammal tissue ref. materials.

- IT 7440-25-7, Tantalum, biological studies  
 7553-56-2, Iodine, biological studies  
 (of frozen whale blubber and liver ref. material)
- RN 7440-25-7 HCA  
 CN Tantalum (8CI, 9CI) (CA INDEX NAME)

Ta

- RN 7553-56-2 HCA  
 CN Iodine (8CI, 9CI) (CA INDEX NAME)

I—I

CC 4-1 (Toxicology)

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104:60191 Reliability of high temperature I2L integrated circuits. Dening, D. C.; LaCombe, D. J.; Christou, A. (Gen.

Electr. Co., Syracuse, NY, 13221, USA). Annual Proceedings - Reliability Physics [Symposium], 22nd, 30-6, 280 (English) 1984. CODEN: ARLPBI. ISSN: 0099-9512.

AB Si-based I<sub>2</sub> L (**integrated** injection logic) **circuits** have survived a life test for over 5000 h at 340.degree. without degrdn. These chips used Al metalization with current densities <10,000 amp/cm<sup>2</sup> to avoid electromigration failures. The need for a Au-based metal system for high temp. applications lead to the development of Ti-w **diffusion barriers** which have withstood temps. of 360.degree. for longer than 3500 h without change. Medium-scale **integrated circuits** with a Ti-W/Au metalization system withstood stress tests of >2000 h at 360.degree.. Au hillock formation is caused by the compressive strains induced in the Au film by thermal expansion mismatches. The driving force for Au hillock formation may be eliminated by depositing the Au film at elevated temps.

CC 76-3 (Electric Phenomena)

ST silicon **integrated circuit** reliability; titanium tungsten gold circuit metalization

IT **Electric circuits**

(**integrated**, injection-logic, silicon, reliability of high-temp.)

IT 12642-02-3

(**diffusion barrier** of, in silicon **integrated** injection logic **circuits**, high-temp. reliability in relation to)

IT 7440-21-3, properties

(**integrated** injection logic **circuits** of, reliability of high-temp.)

IT 7440-57-5, properties

(metalization of, on silicon **integrated** injection logic **circuits**, high-temp. reliability in relation to)

L232 ANSWER 9 OF 9 HCA COPYRIGHT 2003 ACS

70:82284 Solid-state electrochemical devices. Argue, Gary R.; Owens, Boone B. (North American Rockwell Corp.). Fr. FR 1510640 19680119, 7 pp. (French). CODEN: FRXXAK. PRIORITY: US 19660211 - 19660801 19660801.

AB While AgI and Ag<sub>3</sub>Si have been proposed as solid-state electrolytes, their low condns. (10-6-10-2 mho/cm. resp. at ambient temp.) have restricted their use. The compds. MAg<sub>4</sub>I<sub>5</sub>, where M = K, Rb, or NH<sub>4</sub>, have ionic condns. .apprx.0.2 mho/cm. and very low electronic condns. MAg<sub>4</sub>I<sub>5</sub> compds. can be made with any proportions of K, Rb, and NH<sub>4</sub>, and up to 50 at. % Cs. Thus the ionic cond. is fairly const. when M varies between 10-80 at. % K and 90-20 at. % Rb. A mixt. of MAg<sub>4</sub>I<sub>5</sub> and MI (or M<sub>2</sub>AgI<sub>3</sub>) with the empirical formula MAg<sub>3</sub>I<sub>4</sub> is prep'd. by low temp. pptn. from ketone solvents. The ease of prepn. justifies the slightly lower cond. of MAg<sub>3</sub>I<sub>4</sub>. Ag-I cells have been studied with Ag anodes, "MAg<sub>3</sub>I<sub>4</sub>" electrolyte, and I-C cathodes. The C in the cathodes (.apprx.70 wt. %) helps current collection. Cathode contact to the exterior circuit is by

**Ta wire.** The anode current collector may be Ag, Ta, or Cu. Alternative cathode materials are V2O5, CsI5, and MI3 (M = Rb, Cs, NH4). Both anode and cathode materials may be mixed with electrolyte to provide better ionic contact. Thus, a Ag-I cell with 6-mm. thick "KAg3I4" electrolyte, 0.125-mm. thick Ag anode, and 20% I-80% C cathode gave 20.5 ma./cm.2 at 0.4 v. and temps. >35.degree.. Open circuit voltage was 0.68 v. (theoretical, 0.687 v.). For another cell, with both C and "RbAg3I4" mixed with the Ag anode material, 70% Ag utilization was obtained. Cu-I batteries were also studied, with "RbAg3I4" electrolyte. A special advantage of the batteries is the large range of operating temps. (-150 to +230.degree.).

IT 7553-56-2, uses and miscellaneous  
(cathodes contg., for solid-state batteries)

RN 7553-56-2 HCA

CN Iodine (8CI, 9CI) (CA INDEX NAME)

I-I

IC H01M

CC 71 (Electric Phenomena)

ST batteries solid state; solid state batteries; silver I batteries;  
iodine Ag batteries; alkali metals batteries; electrochem  
devices

IT Cathodes  
(battery, iodine-contg. solid-state primary)

IT Batteries, primary  
(solid-state, contg. alkali metal silver iodides)

IT Potassium silver iodide (Ag3KI4)  
Rubidium silver iodide (Ag3RbI4)  
(elec. batteries contg.)

IT 7553-56-2, uses and miscellaneous  
(cathodes contg., for solid-state batteries)